ANALOG DEVICES

Hot Swappable, Dual I²C Isolators

Data Sheet

ADuM1251

FEATURES

Bidirectional I²C communication
Open-drain interfaces
Suitable for hot swap applications
30 mA current sink capability
1000 kHz operation
3.0 V to 5.5 V supply/logic levels
8-lead, RoHS compliant SOIC package
High temperature operation: 125°C
Qualified for automotive applications
Safety and regulatory approvals
- **UL recognition**
  - **2500 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice 5A**
- **VDE certificate of conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
  - **V_{IORM} = 560 V peak**

APPLICATIONS

Isolated I²C, SMBus, or PMBus interfaces
Multilevel I²C interfaces
Power supplies
Networking
Power over Ethernet
Hybrid electric vehicle battery management

FUNCTIONAL BLOCK DIAGRAMS

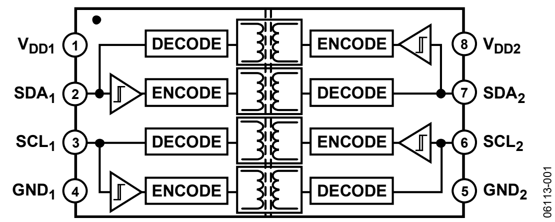

Figure 1. ADuM1250

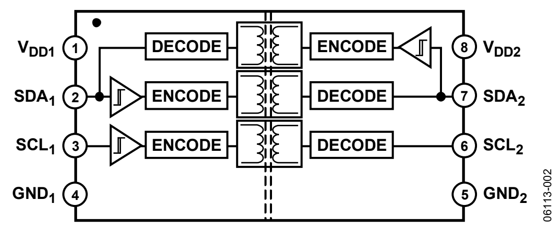

Figure 2. ADuM1251

GENERAL DESCRIPTION

The ADuM1250/ADuM1251[1] are hot swappable digital isolators with nonlatching, bidirectional communication channels that are compatible with I²C interfaces. This eliminates the need for splitting I²C signals into separate transmit and receive signals for use with standalone optocouplers.

The ADuM1250 provides two bidirectional channels, supporting a complete isolated I²C interface. The ADuM1251 provides one bidirectional channel and one unidirectional channel for applications where a bidirectional clock is not required.

Both the ADuM1250 and the ADuM1251 contain hot swap circuitry to prevent glitching data when an unpowered card is inserted onto an active bus.

These isolators are based on the *i*Coupler® chip scale transformer technology from Analog Devices, Inc. *i*Coupler is a magnetic isolation technology with functional, performance, size, and power consumption advantages as compared to optocouplers. With the ADuM1250/ADuM1251, *i*Coupler channels can be integrated with semiconductor circuitry, which enables a complete isolated I²C interface to be implemented in a small form factor.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. I **Document Feedback**

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

DC Specifications[1]

All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V or 5 V, and V_{DD2} = 3.3 V or 5 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1250						
Input Supply Current, Side 1, 5 V	I_{DD1}		2.8	5.0	mA	V_{DD1} = 5 V
Input Supply Current, Side 2, 5 V	I_{DD2}		2.7	5.0	mA	V_{DD2} = 5 V
Input Supply Current, Side 1, 3.3 V	I_{DD1}		1.9	3.0	mA	V_{DD1} = 3.3 V
Input Supply Current, Side 2, 3.3 V	I_{DD2}		1.7	3.0	mA	V_{DD2} = 3.3 V
ADuM1251						
Input Supply Current, Side 1, 5 V	I_{DD1}		2.8	6.0	mA	V_{DD1} = 5 V
Input Supply Current, Side 2, 5 V	I_{DD2}		2.5	4.7	mA	V_{DD2} = 5 V
Input Supply Current, Side 1, 3.3 V	I_{DD1}		1.8	3.0	mA	V_{DD1} = 3.3 V
Input Supply Current, Side 2, 3.3 V	I_{DD2}		1.6	2.8	mA	V_{DD2} = 3.3 V
LEAKAGE CURRENTS	I_{SDA1}, I_{SDA2}, I_{SCL1}, I_{SCL2}		0.01	10	µA	$V_{SDA1} = V_{DD1}$, $V_{SDA2} = V_{DD2}$, $V_{SCL1} = V_{DD1}$, $V_{SCL2} = V_{DD2}$
SIDE 1 LOGIC LEVELS						
Logic Input Threshold[2]	V_{SDA1T}, V_{SCL1T}	500		700	mV	
Logic Low Output Voltages	V_{SDA1OL}, V_{SCL1OL}	600		900	mV	$I_{SDA1} = I_{SCL1}$ = 3.0 mA
		600		850	mV	$I_{SDA1} = I_{SCL1}$ = 0.5 mA
Input/Output Logic Low Level Difference[3]	ΔV_{SDA1}, ΔV_{SCL1}	50			mV	
SIDE 2 LOGIC LEVELS						
Logic Low Input Voltage	V_{SDA2IL}, V_{SCL2IL}			0.3 V_{DD2}	V	
Logic High Input Voltage	V_{SDA2IH}, V_{SCL2IH}	0.7 V_{DD2}			V	
Logic Low Output Voltage	V_{SDA2OL}, V_{SCL2OL}			400	mV	$I_{SDA2} = I_{SCL2}$ = 30 mA

[1] All voltages are relative to their respective ground.
[2] V_{IL} < 0.5 V, V_{IH} > 0.7 V.
[3] $\Delta V_{S1} = V_{S1OL} - V_{S1T}$. This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the part latching up the bus to which it is connected.

AC Specifications[1]

All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V or 5 V, and V_{DD2} = 3.3 V or 5 V, unless otherwise noted. Refer to Figure 5.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM FREQUENCY		1000			kHz	
OUTPUT FALL TIME						
5 V Operation						4.5 V ≤ V_{DD1}, V_{DD2} ≤ 5.5 V, C_{L1} = 40 pF, R1 = 1.6 kΩ, C_{L2} = 400 pF, R2 = 180 Ω
Side 1 Output (0.9 V_{DD1} to 0.9 V)	t_{f1}	13	26	120	ns	
Side 2 Output (0.9 V_{DD2} to 0.1 V_{DD2})	t_{f2}	32	52	120	ns	
3 V Operation						3.0 V ≤ V_{DD1}, V_{DD2} ≤ 3.6 V, C_{L1} = 40 pF, R1 = 1.0 kΩ, C_{L2} = 400 pF, R2 = 120 Ω
Side 1 Output (0.9 V_{DD1} to 0.9 V)	t_{f1}	13	32	120	ns	
Side 2 Output (0.9 V_{DD2} to 0.1 V_{DD2})	t_{f2}	32	61	120	ns	
PROPAGATION DELAY						
5 V Operation						4.5 ≤ V_{DD1}, V_{DD2} ≤ 5.5 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.6 kΩ, R2 = 180 Ω
Side 1 to Side 2, Rising Edge[2]	t_{PLH12}		95	130	ns	
Side 1 to Side 2, Falling Edge[3]	t_{PHL12}		162	275	ns	
Side 2 to Side 1, Rising Edge[4]	t_{PLH21}		31	70	ns	
Side 2 to Side 1, Falling Edge[5]	t_{PHL21}		85	155	ns	
3 V Operation						3.0 V ≤ V_{DD1}, V_{DD2} ≤ 3.6 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.0 kΩ, R2 = 120 Ω
Side 1 to Side 2, Rising Edge[2]	t_{PLH12}		82	125	ns	
Side 1 to Side 2, Falling Edge[3]	t_{PHL12}		196	340	ns	
Side 2 to Side 1, Rising Edge[4]	t_{PLH21}		32	75	ns	
Side 2 to Side 1, Falling Edge[5]	t_{PHL21}		110	210	ns	
PULSE WIDTH DISTORTION						
5 V Operation						4.5 V ≤ V_{DD1}, V_{DD2} ≤ 5.5 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.6 kΩ, R2 = 180 Ω
Side 1 to Side 2, $\|t_{PLH12} - t_{PHL12}\|$	PWD_{12}		67	145	ns	
Side 2 to Side 1, $\|t_{PLH21} - t_{PHL21}\|$	PWD_{21}		54	85	ns	
3 V Operation						3.0 V ≤ V_{DD1}, V_{DD2} ≤ 3.6 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.0 kΩ, R2 = 120 Ω
Side 1 to Side 2, $\|t_{PLH12} - t_{PHL12}\|$	PWD_{12}		114	215	ns	
Side 2 to Side 1, $\|t_{PLH21} - t_{PHL21}\|$	PWD_{21}		77	135	ns	
COMMON-MODE TRANSIENT IMMUNITY[6]	$\|CM_H\|$, $\|CM_L\|$	25	35		kV/µs	

[1] All voltages are relative to their respective ground.
[2] t_{PLH12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.7 V_{DD2}.
[3] t_{PHL12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.4 V.
[4] t_{PLH21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.7 V_{DD1}.
[5] t_{PHL21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.9 V.
[6] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction to Case Thermal Resistance, Side 1	$θ_{JCI}$		46		°C/W	Thermocouple located at center of package underside
IC Junction to Case Thermal Resistance, Side 2	$θ_{JCO}$		41		°C/W	

[1] The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM1250/ADuM1251 have been approved by the organizations listed in Table 4.

Table 4.

UL	CSA	CQC	VDE
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Approved under CQC11-471543-2012	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single/Basic 2500 V rms Isolation Voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 125 V rms (177 V peak) maximum working voltage Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Basic insulation per GB4943.1-2011, 400 V rms (566 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m	Reinforced insulation, 560 V peak
File E214100	File 205078	File CQC14001108691	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM1250/ADuM1251 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM1250/ADuM1251 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)
Maximum Working Voltage Compatible with 50 Year Service Life	V_{IORM}	565	V peak	Continuous peak voltage across the isolation barrier

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input to Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	V_{TR}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
$V_{DD1} + V_{DD2}$ Current		I_{TMAX}	212	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

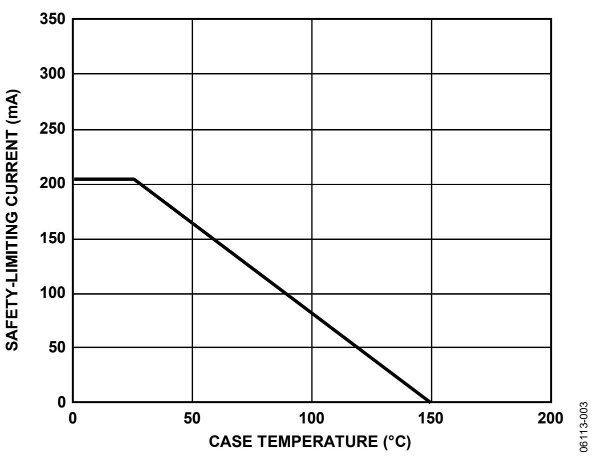

Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Rating
Operating Temperature (T_A)	
A Grade	−40°C to +105°C
S Grade	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	3.0 V to 5.5 V
Input/Output Signal Voltage (V_{SDA1}, V_{SCL1}, V_{SDA2}, V_{SCL2})	5.5 V
Capacitive Load	
Side 1 (C_{L1})	40 pF
Side 2 (C_{L2})	400 pF
Static Output Loading	
Side 1 (I_{SDA1}, I_{SCL1})	0.5 mA to 3 mA
Side 2 (I_{SDA2}, I_{SCL2})	0.5 mA to 30 mA

[1] All voltages are relative to their respective ground. See the Magnetic Field Immunity section for information about immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	
A Grade	−40°C to +105°C
S Grade	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input/Output Voltage,	
Side 1 (V_{SDA1}, V_{SCL1})[2]	−0.5 V to V_{DD1} + 0.5 V
Side 2 (V_{SDA2}, V_{SCL2})[2]	−0.5 V to + 7.0 V
Average Output Current per Pin[2]	
Side 1 (I_{O1})	±18 mA
Side 2 (I_{O2})	±100 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] See Figure 3 for maximum rated current values for various temperatures.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

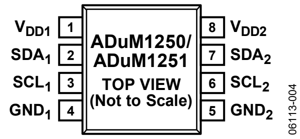

Figure 4. ADuM1250/ADuM1251 Pin Configuration

Table 9. ADuM1250 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage, 3.0 V to 5.5 V.
2	SDA_1	Data Input/Output, Side 1.
3	SCL_1	Clock Input/Output, Side 1.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Isolated ground reference for Isolator Side 2.
6	SCL_2	Clock Input/Output, Side 2.
7	SDA_2	Data Input/Output, Side 2.
8	V_{DD2}	Supply Voltage, 3.0 V to 5.5 V.

Table 10. ADuM1251 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage, 3.0 V to 5.5 V.
2	SDA_1	Data Input/Output, Side 1.
3	SCL_1	Clock Input, Side 1.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Isolated ground reference for Isolator Side 2.
6	SCL_2	Clock Output, Side 2.
7	SDA_2	Data Input/Output, Side 2.
8	V_{DD2}	Supply Voltage, 3.0 V to 5.5 V.

TEST CONDITIONS

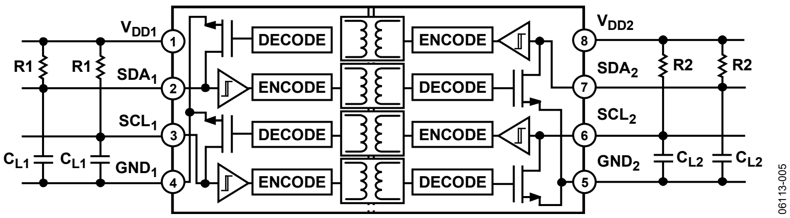

Figure 5. Timing Test Diagram

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The ADuM1250/ADuM1251 interface on each side to a bidirectional I²C signal. Internally, the I²C interface is split into two unidirectional channels communicating in opposing directions via a dedicated *i*Coupler isolation channel for each. One channel (the bottom channel of each channel pair shown in Figure 6) senses the voltage state of the Side 1 I²C pin and transmits its state to its respective Side 2 I²C pin.

Both the Side 1 and the Side 2 I²C pins are designed to interface to an I²C bus operating in the 3.0 V to 5.5 V range. A logic low on either pin causes the opposite pin to be pulled low enough to comply with the logic low threshold requirements of other I²C devices on the bus. Avoidance of I²C bus contention is ensured by an input low threshold at SDA_1 or SCL_1 guaranteed to be at least 50 mV less than the output low signal at the same pin. This prevents an output logic low at Side 1 being transmitted back to Side 2 and pulling down the I²C bus.

Because the Side 2 logic levels/thresholds are standard I²C values, multiple ADuM1250/ADuM1251 devices connected to a bus by their Side 2 pins can communicate with each other and with other I²C compatible devices. A distinction is made between I²C compatibility and I²C compliance. I²C compatibility refers to situations in which the logic levels of a component do not necessarily meet the requirements of the I²C specification but still allow the component to communicate with an I²C compliant device. I²C compliance refers to situations in which the logic levels of a component meet the requirements of the I²C specification.

However, because the Side 1 pin has a modified output level/input threshold, this side of the ADuM1250/ADuM1251 can communicate only with devices that conform to the I²C standard. In other words, Side 2 of the ADuM1250/ADuM1251 is I²C compliant, whereas Side 1 is only I²C compatible.

The output logic low levels are independent of the V_{DD1} and V_{DD2} voltages. The input logic low threshold at Side 1 is also independent of V_{DD1}. However, the input logic low threshold at Side 2 is designed to be at 0.3 V_{DD2}, consistent with I²C requirements. The Side 1 and Side 2 pins have open-collector outputs whose high levels are set via pull-up resistors to their respective supply voltages.

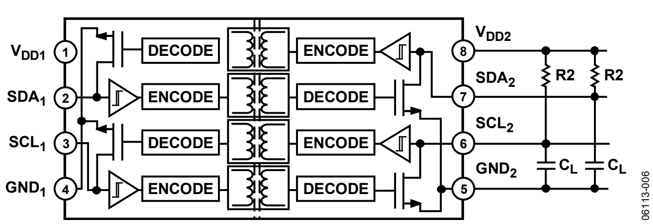

Figure 6. ADuM1250 Block Diagram

STARTUP

Both the V_{DD1} and V_{DD2} supplies have an undervoltage lockout feature to prevent the signal channels from operating unless certain criteria are met. This feature prevents input logic low signals from pulling down the I²C bus inadvertently during power-up/power-down.

For the signal channels to be enabled, the following two criteria must be met:

- Both supplies must be at least 2.5 V.
- At least 40 µs must elapse after both supplies exceed the internal startup threshold of 2.0 V.

Until both criteria are met for both supplies, the ADuM1250/ADuM1251 outputs are pulled high, ensuring a startup that avoids any disturbances on the bus. Figure 7 and Figure 8 illustrate the supply conditions for fast and slow input supply slew rates.

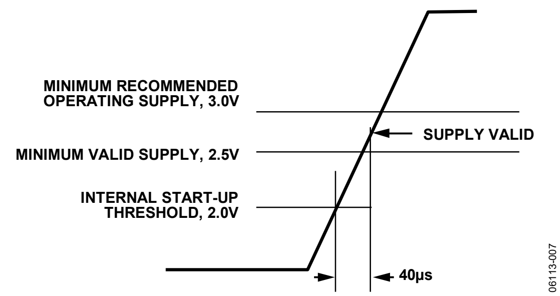

Figure 7. Start-Up Condition, Supply Slew Rate > 12.5 V/ms

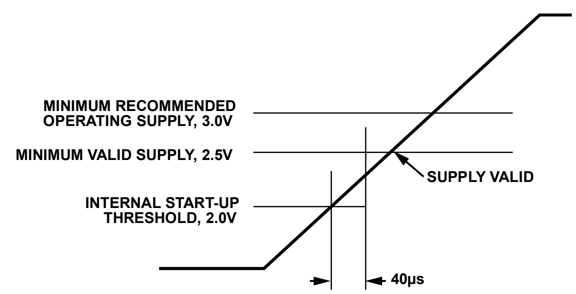

Figure 8. Start-Up Condition, Supply Slew Rate < 12.5 V/ms

TYPICAL APPLICATION DIAGRAM

Figure 9 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2 buses. Bypass capacitors with values from 0.01 µF to 0.1 µF are required between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The 200 Ω resistor shown in Figure 9 is required for latch-up immunity if the ambient temperature can be between 105°C and 125°C.

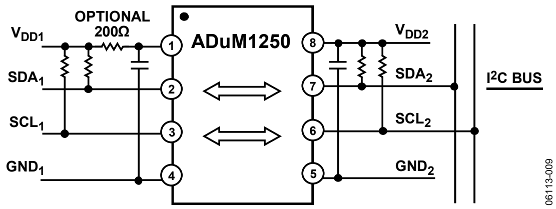

Figure 9. Typical Isolated I²C Interface Using the ADuM1250

CAPACITIVE LOAD AT LOW SPEEDS

The ADuM1250/ADuM1251 are designed for operation at speeds up to 1 Mbps. Due to the limited current available on Side 1, operation at 1 Mbps limits the capacitance that can be driven at the minimum pull-up value to 40 pF.

Most applications operate at 100 kbps in standard mode or 400 kbps in fast mode. At these lower operating speeds, the limitation on the load capacitance can be significantly relaxed. Table 11 shows the maximum capacitance at minimum pull-up values for standard and fast operating modes. If larger values for the pull up resistor are used, the maximum supported capacitance must be scaled down proportionally so that the rise time does not increase beyond the values required by the standard.

Table 11. Side 1 Maximum Load Conditions

Maximum Capacitive Load for Side 1						
Mode	**V_{DD1}**	**Data Rate (kbps)**	**t_r (ns)**	**t_f (ns)**	**R_1 (Ω)**	**C_{L1} (pF)**
Standard	5	100	1000	187	1600	484
Fast	5	400	300	172	1600	120
Standard	3.3	100	1000	270	1000	771
Fast	3.3	400	300	235	1000	188

MAGNETIC FIELD IMMUNITY

The ADuM1250/ADuM1251 are extremely immune to external magnetic fields. The limitation on the magnetic field immunity of the ADuM1250/ADuM1251 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM1250/ADuM1251 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the total number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1250/ADuM1251 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 10.

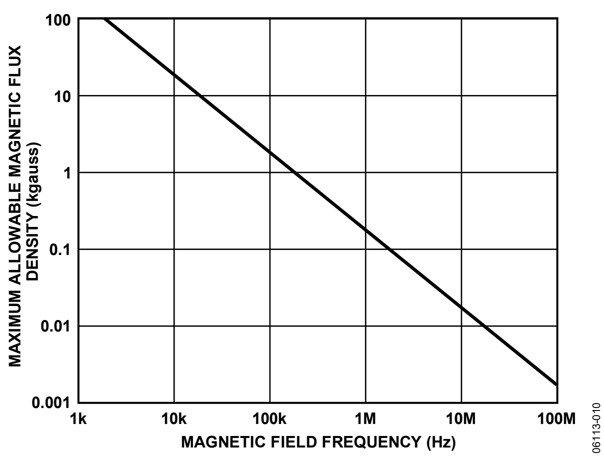

Figure 10. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1250/ADuM1251 transformers. Figure 11 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 11, the ADuM1250/ADuM1251 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current placed 5 mm away from the ADuM1250/ADuM1251 is required to affect the operation of the component.

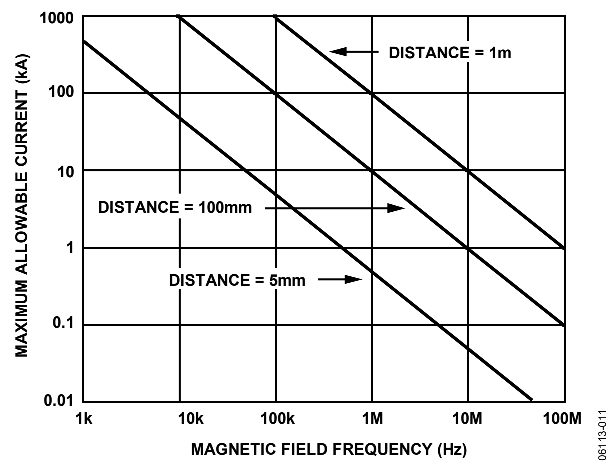

Figure 11. Maximum Allowable Current for Various Current-to-ADuM1250/ADuM1251 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

OUTLINE DIMENSIONS

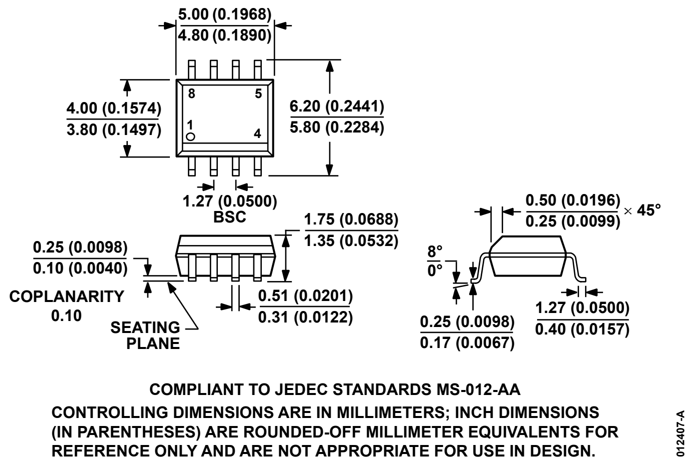

Figure 12. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay (ns)	Temperature Range	Package Description	Package Option
ADuM1250ARZ	2	2	1	150	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM1250ARZ-RL7	2	2	1	150	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM1250SRZ	2	2	1	150	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM1250SRZ-RL7	2	2	1	150	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM1250WSRZ	2	2	1	150	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM1250WSRZ-RL7	2	2	1	150	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM1251ARZ	2	1	1	150	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM1251ARZ-RL7	2	1	1	150	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM1251WARZ	2	1	1	150	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM1251WARZ-RL7	2	1	1	150	−40°C to +125°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADuM1250W and ADuM1251W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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