11.3 Gbps, Active Back-Termination, Differential VCSEL Driver

Data Sheet

ADN2530

FEATURES

Up to 11.3 Gbps operation
−40°C to +100°C operation
Very low power: I_{SUPPLY} = 65 mA
Typical 26 ps rise/fall times
Full back-termination of output transmission lines
Crosspoint adjust function
PECL-/CML-compatible data inputs
Bias current range: 2 mA to 25 mA
Differential modulation current range: 2.2 mA to 23 mA
Automatic laser shutdown (ALS)
3.3 V operation
Compact 3 mm × 3 mm LFCSP
Voltage-input control for bias and modulation currents
XFP-compliant bias current monitor

APPLICATIONS

10 Gb Ethernet optical transceivers
10G-BASE-LRM optical transceivers
8× and 10× Fibre Channel optical transceivers
XFP/X2/XENPAK/MSA 300 optical modules
SONET OC-192/SDH STM-64 optical transceivers

GENERAL DESCRIPTION

The ADN2530 laser diode driver is designed for direct modulation of packaged VCSELs with a differential resistance ranging from 35 Ω to 140 Ω. The active back-termination technique provides excellent matching with the output transmission lines while reducing the power dissipation in the output stage. The back-termination in the ADN2530 absorbs signal reflections from the TOSA end of the output transmission lines, enabling excellent optical eye quality to be achieved even when the TOSA end of the output transmission lines is significantly misterminated. The small package provides the optimum solution for compact modules where laser diodes are packaged in low pin count optical subassemblies.

The modulation and bias currents are programmable via the MSET and BSET control pins. By driving these pins with control voltages, the user has the flexibility to implement various average power and extinction ratio control schemes, including closed-loop control and look-up tables. The eye crosspoint in the output eye diagram is adjustable via the crosspoint adjust (CPA) control voltage input. The automatic laser shutdown (ALS) feature allows the user to turn on/off the bias and modulation currents by driving the ALS pin with the proper logic levels. The product is available in a space-saving 3 mm × 3 mm LFCSP specified from −40°C to +100°C.

FUNCTIONAL BLOCK DIAGRAM

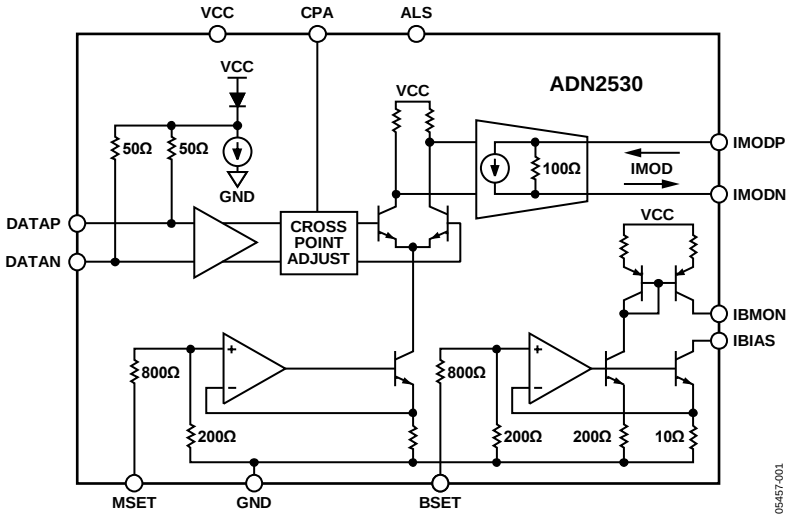

Figure 1.

Document Feedback

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REVISION HISTORY

7/2017—Rev. C to Rev. D

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10/2013—Rev. A to Rev. B

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8/2006—Rev. 0 to Rev. A

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10/2005—Revision 0: Initial Version

SPECIFICATIONS

VCC = VCC_{MIN} to VCC_{MAX}, T_A = −40°C to +100°C, 100 Ω differential load impedance, crosspoint adjust disabled, unless otherwise noted. Typical values are specified at 25°C and IMOD = 10 mA with crosspoint adjust disabled, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BIAS CURRENT (IBIAS)					
Bias Current Range	2		25	mA	
Bias Current While ALS Asserted			50	µA	ALS = high
Compliance Voltage[1]	0.55		VCC − 1.3	V	IBIAS = 25 mA
	0.55		VCC − 0.8	V	IBIAS = 2 mA
MODULATION CURRENT (IMODP, IMODN)					
Modulation Current Range	2.2		23	mA diff	R_{LOAD} = 35 Ω to 100 Ω differential
	2.2		19	mA diff	R_{LOAD} = 140 Ω differential
Modulation Current While ALS Asserted			250	µA diff	ALS = high
Crosspoint Adjust (CPA) Range[2]	35		65	%	
Rise Time (20% to 80%)[2, 3, 4]		26	32.5	ps	CPA disabled
		26.4	34.7	ps	CPA 35% to 65%
Fall Time (20% to 80%)[2, 3, 4]		26	32.5	ps	CPA disabled
		26.5	33.7	ps	CPA 35% to 65%
Random Jitter[2, 3, 4]		<0.5		ps rms	CPA disabled
		<0.5		ps rms	CPA 35% to 65%
Deterministic Jitter[2, 4, 5]		5.4	8.2	ps p-p	10.7 Gbps, CPA disabled
		5.8	8.2	ps p-p	10.7 Gbps, CPA 35% to 65%
Deterministic Jitter[2, 4, 6]		5.4	8.2	ps p-p	11.3 Gbps, CPA disabled
		5.8	8.2	ps p-p	11.3 Gbps, CPA 35% to 65%
Differential |S22|		−5		dB	5 GHz < f < 10 GHz, Z_0 = 100 Ω differential
		−13.6		dB	f < 5 GHz, Z_0 = 100 Ω differential
Compliance Voltage[1]	VCC − 0.7		VCC + 0.7	V	
DATA INPUTS (DATAP, DATAN)					
Input Data Rate			11.3	Gbps	NRZ
Differential Input Swing	0.4		1.6	V p-p diff	Differential ac-coupled
Differential |S11|		−15		dB	f < 10 GHz, Z_0 = 100 Ω differential
Input Termination Resistance	85	100	115	Ω	Differential
BIAS CONTROL INPUT (BSET)					
BSET Voltage to IBIAS Gain	15	20	24	mA/V	
BSET Input Resistance	800	1000	1200	Ω	
MODULATION CONTROL INPUT (MSET)					
MSET Voltage to IMOD Gain	14	19	23	mA/V	
MSET Input Resistance	800	1000	1200	Ω	
BIAS MONITOR (IBMON)					
IBMON to IBIAS Ratio		50		µA/mA	
Accuracy of IBIAS to IBMON Ratio	−5.0		+5.0	%	IBIAS = 2 mA, R_{IBMON} = 750 Ω
	−4.3		+4.3	%	IBIAS = 4 mA, R_{IBMON} = 750 Ω
	−3.5		+3.5	%	IBIAS = 8 mA, R_{IBMON} = 750 Ω
	−3.0		+3.0	%	IBIAS = 14 mA, R_{IBMON} = 750 Ω
	−2.5		+2.5	%	IBIAS = 25 mA, R_{IBMON} = 750 Ω
AUTOMATIC LASER SHUTDOWN (ALS)					
V_{IH}	2.4			V	
V_{IL}			0.8	V	
I_{IL}	−20		+20	µA	
I_{IH}	0		200	µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ALS Assert Time			2	µs	Rising edge of ALS to fall of IBIAS and IMOD below 10% of nominal; see Figure 2
ALS Negate Time			10	µs	Falling edge of ALS to rise of IBIAS and IMOD above 90% of nominal; see Figure 2
POWER SUPPLY					
V_{CC}	3.07	3.3	3.53	V	
I_{CC}[7]		27	32	mA	$V_{BSET} = V_{MSET} = 0$ V
I_{SUPPLY}[8]		65	76	mA	$V_{BSET} = V_{MSET} = 0$ V

[1] The voltage between the pin with the specified compliance voltage and GND.
[2] Specified for $T_A = -40°C$ to $+85°C$ due to test equipment limitation. See the Typical Performance Characteristics section for data on performance for $T_A = -40°C$ to $+100°C$.
[3] The pattern used is composed of a repetitive sequence of eight 1s followed by eight 0s at 10.7 Gbps.
[4] Measured using the high speed characterization circuit shown in Figure 3.
[5] The pattern used is K28.5 (0011111010110000010l) at 10.7 Gbps rate.
[6] The pattern used is K28.5 (0011111010110000010l) at 11.3 Gbps rate.
[7] Only includes current in the ADN2530 VCC pins.
[8] Includes current in ADN2530 VCC pins and dc current in IMODP and IMODN pull-up inductors. See the Power Consumption section for total supply current calculation.

PACKAGE THERMAL SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
$\theta_{J\text{-}TOP}$	65	72.2	79.4	°C/W	Thermal resistance from junction to top of package.
$\theta_{J\text{-}PAD}$	2.6	5.8	10.7	°C/W	Thermal resistance from junction to bottom of exposed pad.
IC Junction Temperature			125	°C	

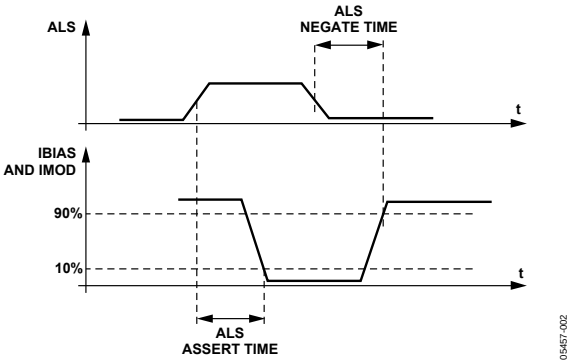

Figure 2. ALS Timing Diagram

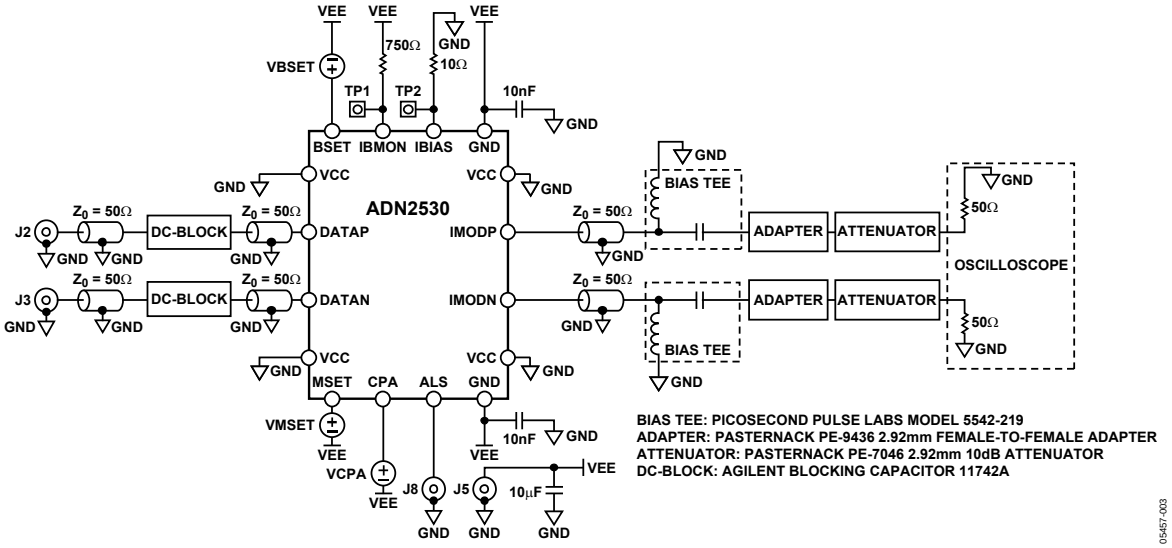

Figure 3. High Speed Characterization Circuit

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VCC to GND	−0.3 V to +4.2 V
IMODP, IMODN to GND	VCC − 1.5 V to +4.5 V
DATAP, DATAN to GND	VCC − 1.8 V to VCC − 0.4 V
All Other Pins	−0.3 V to VCC + 0.3 V
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Soldering Temperature (<10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

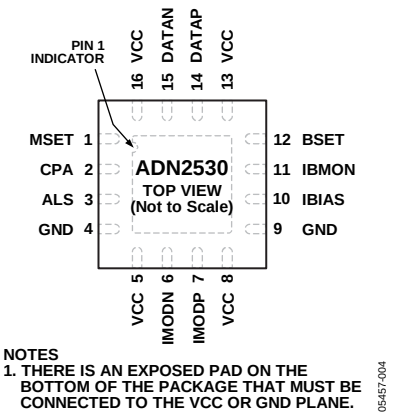

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output/Power	Description
1	MSET	Input	Modulation Current Control Input
2	CPA	Input	Crosspoint Adjust Control Input
3	ALS	Input	Automatic Laser Shutdown
4	GND	Power	Negative Power Supply
5	VCC	Power	Positive Power Supply
6	IMODN	Output	Modulation Current Negative Output
7	IMODP	Output	Modulation Current Positive Output
8	VCC	Power	Positive Power Supply
9	GND	Power	Negative Power Supply
10	IBIAS	Output	Bias Current Output
11	IBMON	Output	Bias Current Monitoring Output
12	BSET	Input	Bias Current Control Input
13	VCC	Power	Positive Power Supply
14	DATAP	Input	Data Signal Positive Input
15	DATAN	Input	Data Signal Negative Input
16	VCC	Power	Positive Power Supply
	EPAD	Power	Connect the Exposed Pad to GND or VCC

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, VCC = 3.3 V, crosspoint adjust disabled, unless otherwise noted.

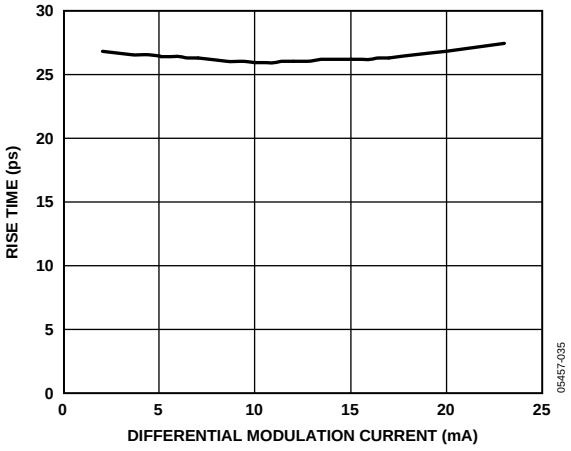

Figure 5. Rise Time vs. IMOD

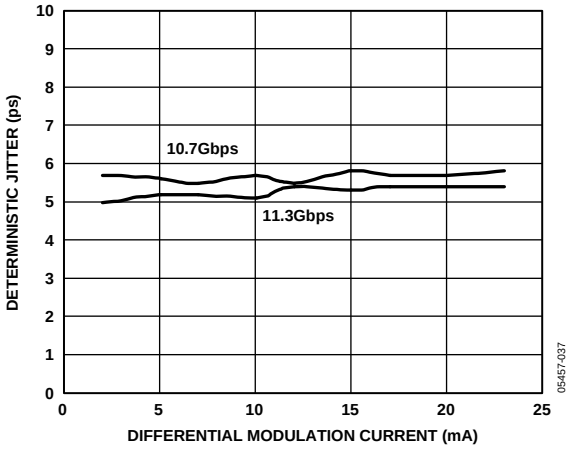

Figure 8. Deterministic Jitter vs. IMOD

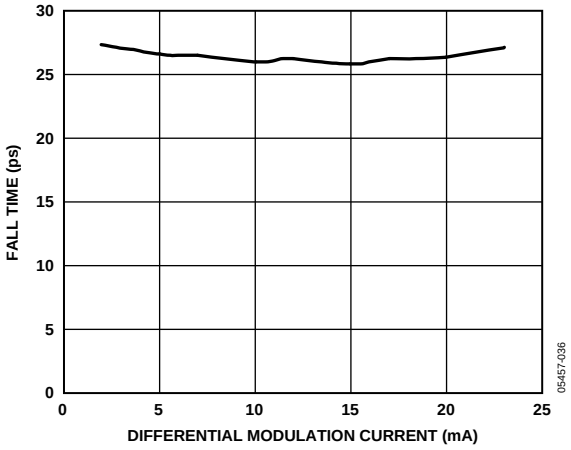

Figure 6. Fall Time vs. IMOD

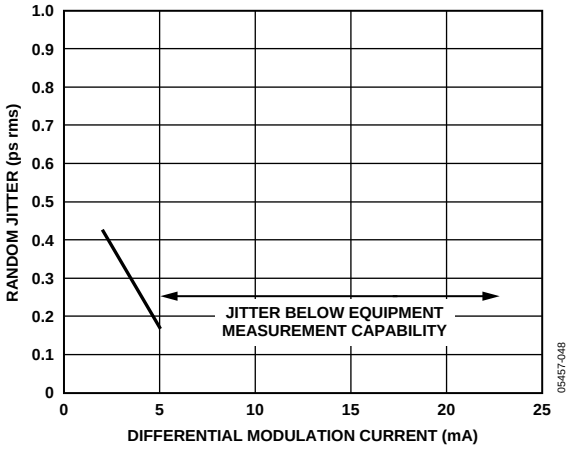

Figure 9. Random Jitter vs. IMOD

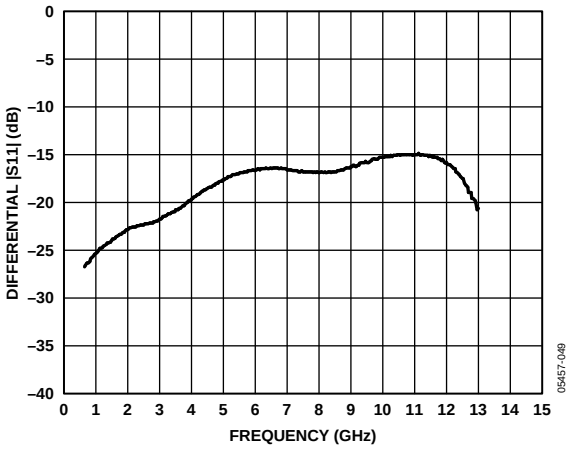

Figure 7. Differential |S11| vs. Frequency

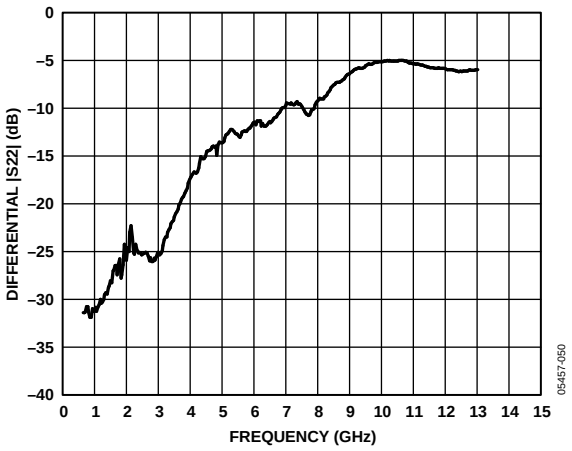

Figure 10. Differential |S22| vs. Frequency

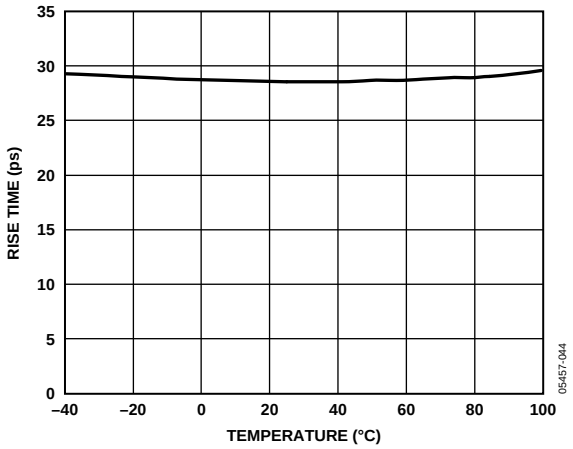

Figure 11. Rise Time vs. Temperature (Worse Case Conditions, CPA Disabled)

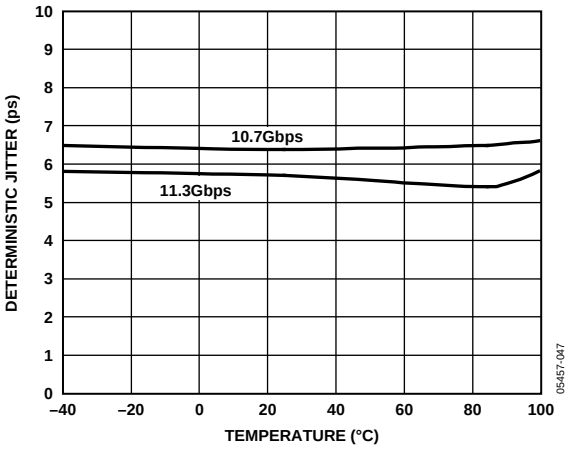

Figure 14. Deterministic Jitter vs. Temperature (Worse Case Conditions, CPA Disabled)

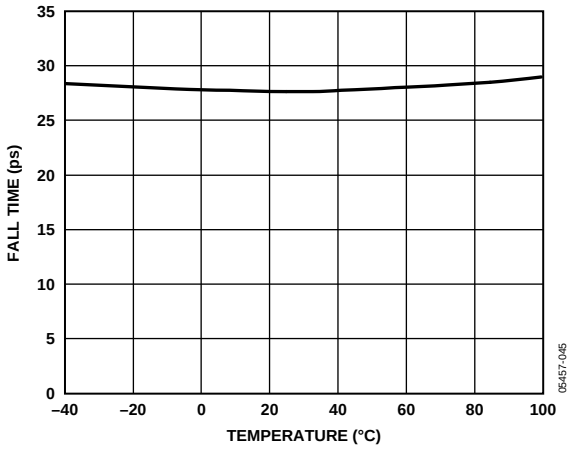

Figure 12. Fall Time vs. Temperature (Worst Case Conditions, CPA Disabled)

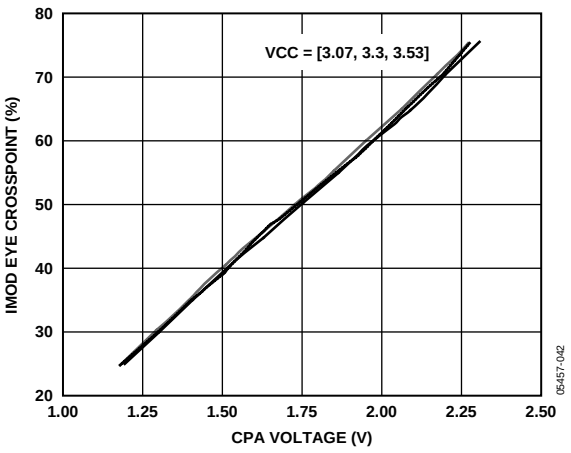

Figure 15. IMOD Eye Diagram Crosspoint vs. CPA Voltage and VCC (IMOD = 10 mA)

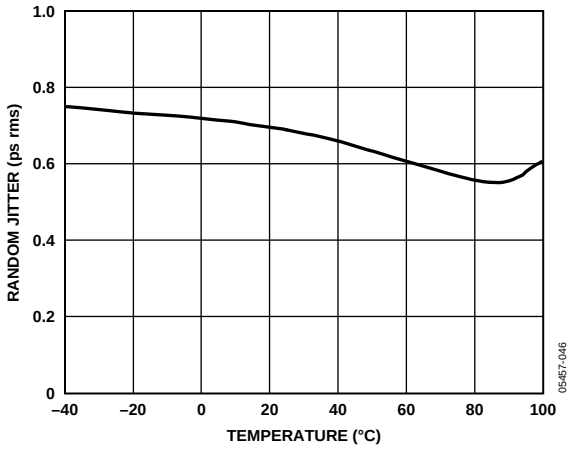

Figure 13. Random Jitter vs. Temperature (Worst Case Conditions, CPA Disabled [Worst Case IMOD = 2.2 mA])

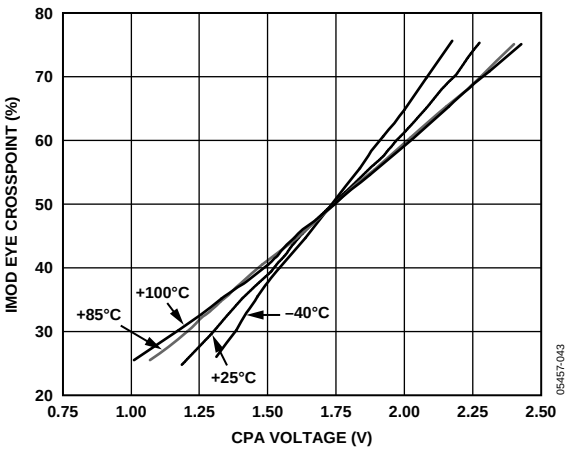

Figure 16. IMOD Eye Diagram Crosspoint vs. CPA Voltage and Temperature (IMOD = 10 mA)

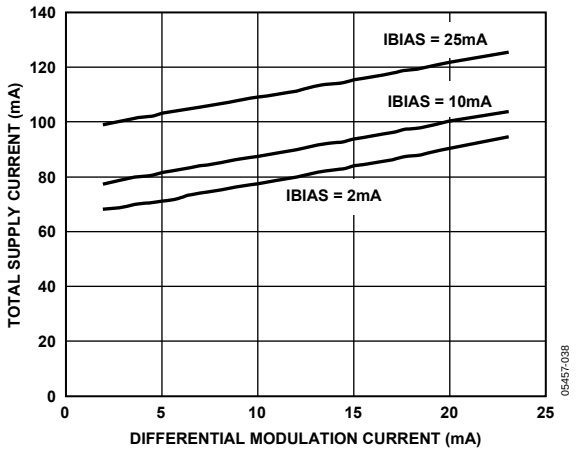

Figure 17. Total Supply Current vs. IMOD

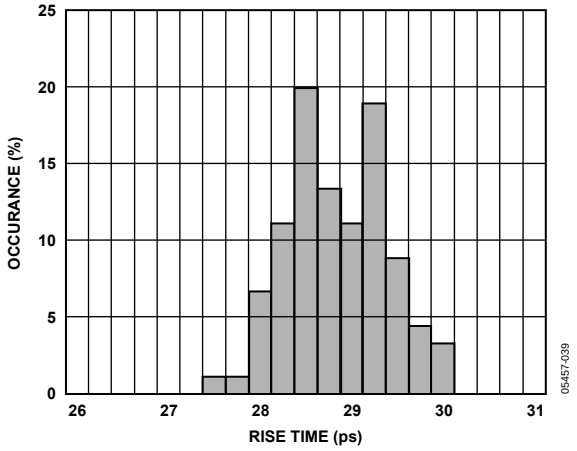

Figure 18. Worst Case Rise Time Distribution

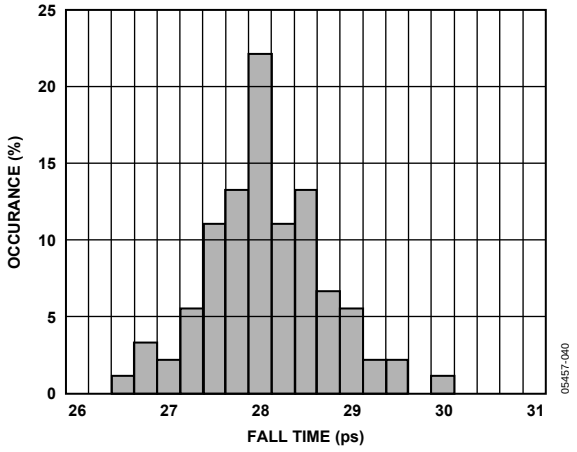

Figure 19. Worst Case Fall Time Distribution

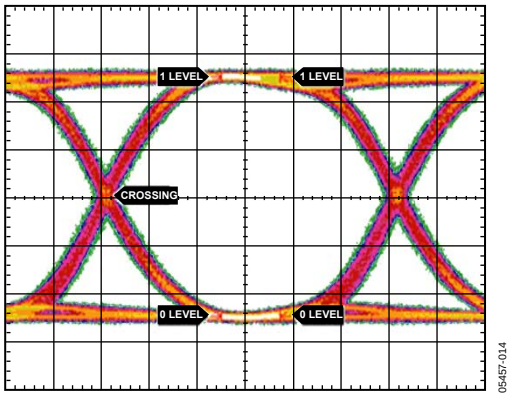

Figure 20. Electrical Eye Diagram
(IMOD = 10 mA, PRBS^{31} Pattern at 10.3125 Gbps)

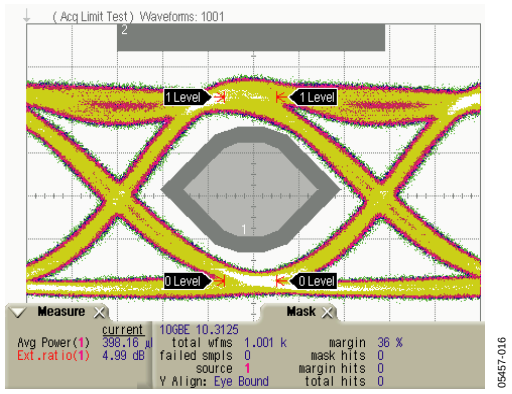

Figure 21. Filtered 10G Ethernet Optical Eye Using AOC HFE6192-562 VCSEL
(PRBS^{31} Pattern at 10.3125 Gbps, 3 dB Optical Attenuator)

THEORY OF OPERATION

As shown in Figure 1, the ADN2530 consists of an input stage and two voltage-controlled current sources for bias and modulation. The bias current is available at the IBIAS pin. It is controlled by the voltage at the BSET pin and can be monitored at the IBMON pin. The differential modulation current is available at the IMODP and IMODN pins. It is controlled by the voltage at the MSET pin. The output stage implements the active back-termination circuitry for proper transmission line matching and power consumption reduction. The ADN2530 can drive a load with differential resistance ranging from 35 Ω to 140 Ω. The excellent back-termination in the ADN2530 absorbs signal reflections from the TOSA end of the output transmission lines, enabling excellent optical eye quality to be achieved even when the TOSA end of the output transmission lines is significantly misterminated.

INPUT STAGE

The input stage of the ADN2530 converts the data signal applied to the DATAP and DATAN pins to a level that ensures proper operation of the high speed switch. The equivalent circuit of the input stage is shown in Figure 22.

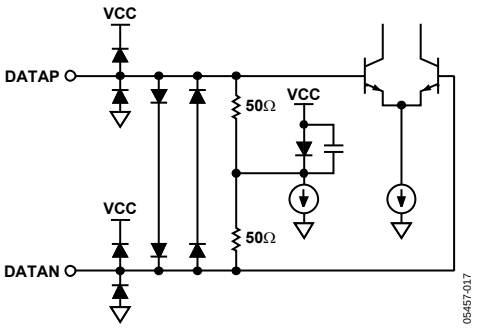

Figure 22. Equivalent Circuit of the Input Stage

The DATAP and DATAN pins are terminated internally with a 100 Ω differential termination resistor. This minimizes signal reflections at the input that could otherwise lead to degradation in the output eye diagram. It is not recommended to drive the ADN2530 with single-ended data signal sources.

The ADN2530 input stage must be ac-coupled to the signal source to eliminate the need for matching between the common-mode voltages of the data signal source and the input stage of the driver (see Figure 23). The ac coupling capacitors must have an impedance less than 50 Ω over the required frequency range. Generally, this is achieved using 10 nF to 100 nF capacitors.

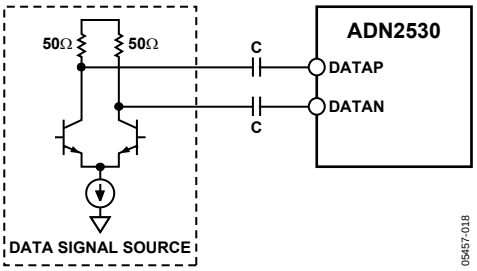

Figure 23. AC Coupling the Data Source to the ADN2530 Data Inputs

BIAS CURRENT

The bias current is generated internally using a voltage to current converter consisting of an internal operational amplifier and a transistor, as shown in Figure 24.

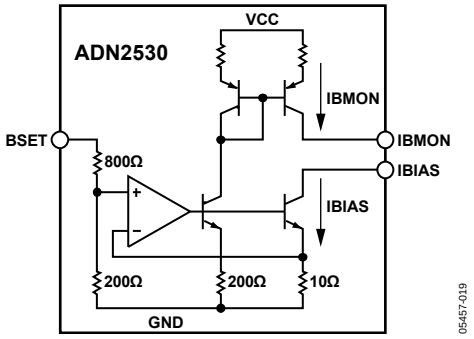

Figure 24. Voltage-to-Current Converter Used to Generate IBIAS

The BSET to IBIAS voltage-to-current conversion factor is set at 20 mA/V by the internal resistors, and the bias current is monitored at the IBMON pin using a current mirror with a gain equal to 1/20. By connecting a 750 Ω resistor between IBMON and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor must be used for the IBMON resistor (R_{IBMON}). Any error in the value of R_{IBMON} due to tolerances or drift in its value over temperature contributes to the overall error budget for the IBIAS monitor voltage. If the IBMON voltage connects to an ADC for analog-to-digital conversion, place R_{IBMON} close to the ADC to minimize errors due to voltage drops on the ground plane. See the Design Example section for example calculations of the accuracy of the IBIAS monitor as a percentage of the nominal IBIAS value.

The equivalent circuits of the BSET, IBIAS, and IBMON pins are shown in Figure 25 to Figure 27.

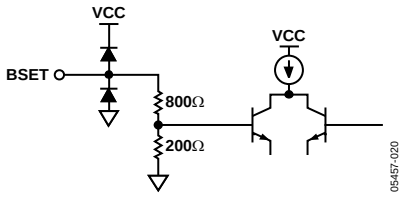

Figure 25. Equivalent Circuit of the BSET Pin

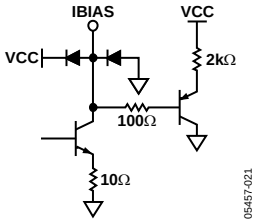

Figure 26. Equivalent Circuit of the IBIAS Pin

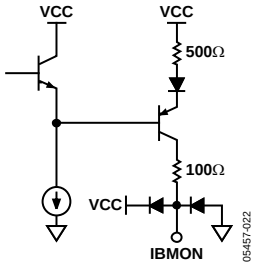

Figure 27. Equivalent Circuit of the IBMON Pin

The recommended configuration for BSET, IBIAS, and IBMON is shown in Figure 28.

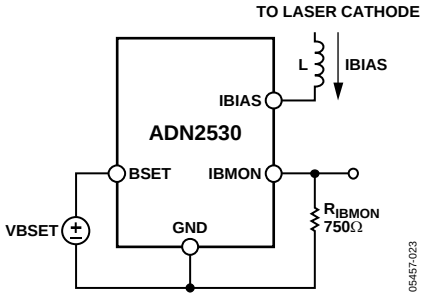

Figure 28. Recommended Configuration for BSET, IBIAS, and IBMON Pins

The circuit used to drive the BSET voltage must be able to drive the 1 kΩ input resistance of the BSET pin. For proper operation of the bias current source, the voltage at the IBIAS pin must be between the compliance voltage specifications for this pin over supply, temperature, and bias current range (see Table 1). The maximum compliance voltage is specified for only two bias current levels (2 mA and 25 mA), but it can be calculated for any bias current by

$$V_{COMPLIANCE}\ (\text{V}) = VCC\ (\text{V}) - 0.75 - 22 \times IBIAS\ (\text{A})$$

See the Headroom Calculations section for examples.

The function of Inductor L is to isolate the capacitance of the IBIAS output from the high frequency signal path. For recommended components, see Table 6.

AUTOMATIC LASER SHUTDOWN (ALS)

The ALS pin is a digital input that enables/disables both the bias and modulation currents, depending on the logic state applied, as shown in Table 5.

Table 5.

ALS Logic State	IBIAS and IMOD
High	Disabled
Low	Enabled
Floating	Enabled

The ALS pin is compatible with 3.3 V CMOS and TTL logic levels. Its equivalent circuit is shown in Figure 29.

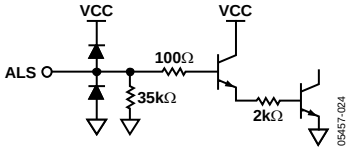

Figure 29. Equivalent Circuit of the ALS Pin

MODULATION CURRENT

The modulation current can be controlled by applying a dc voltage to the MSET pin. This voltage is converted into a dc current by using a voltage-to-current converter that uses an operational amplifier and a bipolar transistor, as shown in Figure 30.

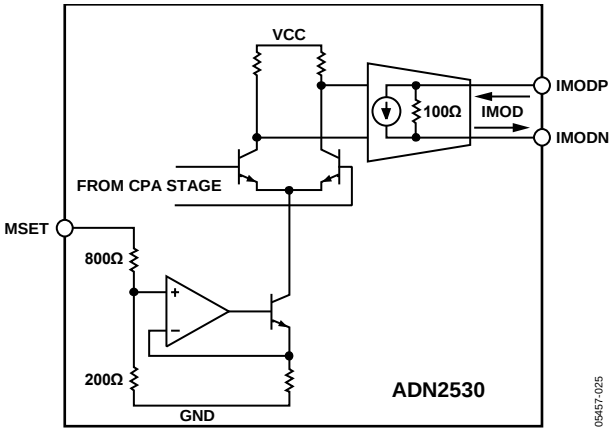

Figure 30. Generation of Modulation Current on the ADN2530

This dc current is switched by the data signal applied to the input stage (DATAP and DATAN pins) and gained up by the output stage to generate the differential modulation current at the IMODP and IMODN pins. The output stage also generates the active back-termination, which provides proper transmission line termination. Active back-termination uses feedback around an active circuit to synthesize a broadband termination resistance.

This provides excellent transmission line termination while dissipating less power than a traditional resistor passive back-termination. No portion of the modulation current flows in the active back-termination resistance. All of the preset modulation current IMOD, the range specified in Table 1, flows in the external load. The equivalent circuits for MSET, IMODP, and IMODN are shown in Figure 31 and Figure 32. The two 50 Ω resistors in Figure 32 are not real resistors. They represent the active back-termination resistance.

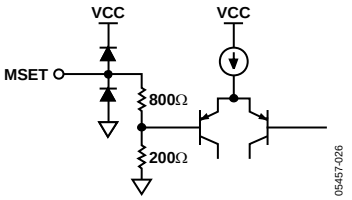

Figure 31. Equivalent Circuit of the MSET Pin

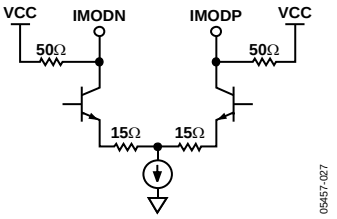

Figure 32. Equivalent Circuit of the IMODP and IMODN Pins

The recommended configuration of the MSET, IMODP, and IMODN pins is shown in Figure 33. See Table 6 for recommended components. When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows into the IMODP pin and out of the IMODN pin, generating an optical Logic 1 level at the TOSA output when the TOSA is connected as shown in Figure 33.

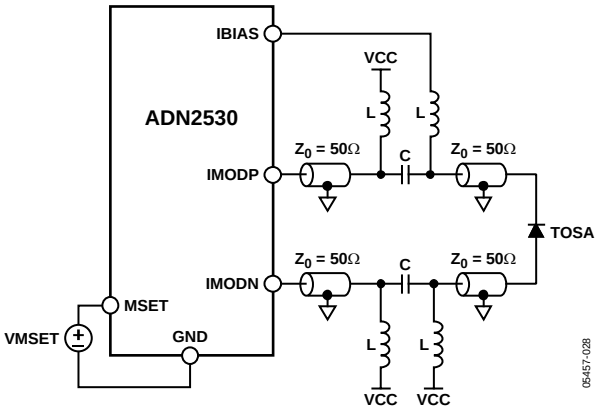

Figure 33. Recommended Configuration for the MSET, IMODP, and IMODN Pins

The ratio between the voltage applied to the MSET pin and the differential modulation current available at the IMODP and IMODN pins is a function of the load resistance value, as shown in Figure 34.

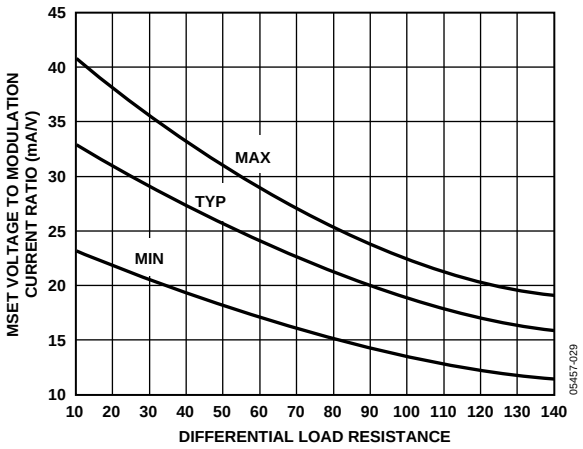

Figure 34. MSET Voltage to Modulation Current Ratio vs. Differential Load Resistance

Using the resistance of the TOSA, the user can calculate the voltage range that should be applied to the MSET pin to generate the required modulation current range (see the example in the Applications Information section).

The circuit used to drive the MSET voltage must be able to drive the 1 kΩ resistance of the MSET pin. To be able to drive 23 mA modulation currents through the differential load, the output stage of the ADN2530 (IMODP and IMODN pins) must be ac-coupled to the load. The voltages at these pins have a dc component equal to VCC and an ac component with single-ended peak-to-peak amplitude of IMOD × 50 Ω. This is the case when the load impedance (R_{TOSA}) is less than 100 Ω differential because the transmission line characteristic impedance sets the peak-to-peak amplitude. For the case where R_{TOSA} is greater than 100 Ω, the single-ended, peak-to-peak amplitude is IMOD × R_{TOSA} ÷ 2. For proper operation of the output stage, the voltages at the IMODP and IMODN pins must be between the compliance voltage specifications for this pin over supply, temperature, and modulation current range, as shown in Figure 35. See the Headroom Calculations section for examples of headroom calculations.

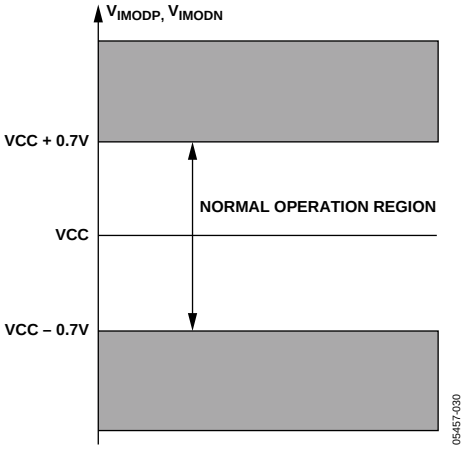

Figure 35. Allowable Range for the Voltage at IMODP and IMODN

LOAD MISTERMINATION

Due to its excellent S22 performance, the ADN2530 can drive differential loads that range from 35 Ω to 140 Ω. In practice, many TOSAs have differential resistance not equal to 100 Ω. In this case, with 100 Ω differential transmission lines connecting the ADN2530 to the load, the load end of the transmission lines are misterminated. This mistermination leads to signal reflections back to the driver. The excellent back-termination in the ADN2530 absorbs these reflections, preventing their reflection back to the load. This enables excellent optical eye quality to be achieved even when the load end of the transmission lines is significantly misterminated. The connection between the load and the ADN2530 must be made with 100 Ω differential (50 Ω single-ended) transmission lines so that the driver end of the transmission lines is properly terminated.

CROSSPOINT ADJUST

The crossing level in the output electrical eye diagram can be adjusted between 35% and 65% using the crosspoint adjust (CPA) control input. This can be used to compensate for asymmetry in the VCSEL response and optimizes the optical eye mask margin. The CPA input is a voltage control input, and a plot of eye crosspoint vs. CPA control voltage is shown in Figure 15 and Figure 16 in the Typical Performance Characteristics section. The equivalent circuit for the CPA pin is shown in Figure 36. To disable the crosspoint adjust function and set the eye crossing to 50%, tie the CPA pin to VCC.

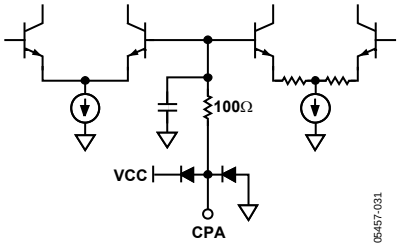

Figure 36. Equivalent Circuit for CPA Pin

POWER CONSUMPTION

The power dissipated by the ADN2530 is given by

$$P = VCC \times \left(\frac{V_{MSET}}{50} + I_{SUPPLY} \right) + V_{IBIAS} \times (IBIAS \times 1.2)$$

where:
VCC is the power supply voltage.
V_{MSET} is the voltage applied to the MSET pin.
I_{SUPPLY} is the sum of the current that flows into the VCC, IMODP, and IMODN pins of the ADN2530 when IBIAS = IMOD = 0 expressed in amps (see Table 1).
V_{IBIAS} is the average voltage on the IBIAS pin.
IBIAS is the bias current generated by the ADN2530.

Considering VBSET/IBIAS = 50 as the conversion factor from V_{BSET} to IBIAS, the dissipated power becomes

$$P = VCC \times \left(\frac{V_{MSET}}{50} + I_{SUPPLY} \right) + V_{IBIAS} \times \left(\frac{V_{BSET}}{50} \times 1.2 \right)$$

To ensure long-term reliable operation, the junction temperature of the ADN2530 must not exceed 125°C, as specified in Table 2. For improved heat dissipation, the module's case can be used as a heat sink, as shown in Figure 37.

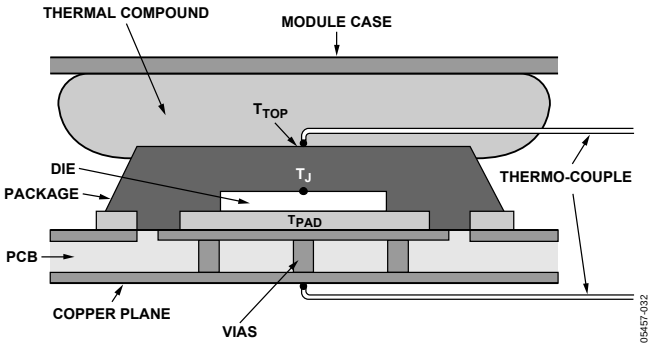

Figure 37. Typical Optical Module Structure

A compact optical module is a complex thermal environment, and calculations of device junction temperature using the package θ_{JA} (junction-to-ambient thermal resistance) do not yield accurate results. Use the following equation, derived from the model in Figure 38, to estimate the IC junction temperature:

$$T_J = \frac{P \times \left(\theta_{J-PAD} \times \theta_{J-TOP}\right) + T_{TOP} \times \theta_{J-PAD} + T_{PAD} \times \theta_{J-TOP}}{\theta_{J-PAD} + \theta_{J-TOP}}$$

where:
T_J is the IC junction temperature in degrees Celsius.
P is the ADN2530 power dissipation in watts.
$\theta_{J\text{-}PAD}$ is the thermal resistance from IC junction to package exposed pad.
$\theta_{J\text{-}TOP}$ is the thermal resistance from IC junction to package top.
T_{TOP} is the temperature at top of package in degrees Celsius.
T_{PAD} is the temperature at package exposed paddle in degrees Celsius.

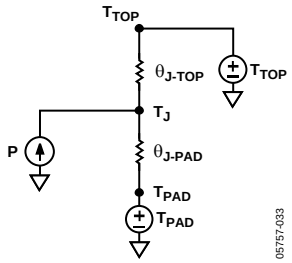

Figure 38. Electrical Model for Thermal Calculations

T_{TOP} and T_{PAD} can be determined by measuring the temperature at points inside the module, as shown in Figure 37. Position the thermocouples to obtain an accurate measurement of the package top and paddle temperatures. $\theta_{J\text{-}TOP}$ and $\theta_{J\text{-}PAD}$ are given in Table 2.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 39 shows the typical application circuit for the ADN2530. The dc voltages applied to the BSET and MSET pins control the bias and modulation currents. The bias current can be monitored as a voltage drop across the 750 Ω resistor connected between the IBMON pin and GND. The dc voltage applied to the CPA pin controls the crosspoint in the output eye diagram. By tying the CPA pin to VCC, the CPA function is disabled. The ALS pin allows the user to turn on/off the bias and modulation currents depending on the logic level applied to the pin. The data signal source must be connected to the DATAP and DATAN pins of the ADN2530 using 50 Ω transmission lines. The modulation current outputs, IMODP and IMODN, must be connected to the load (TOSA) using 100 Ω differential (50 Ω single-ended) transmission lines. Table 6 shows recommended components for the ac-coupling interface between the ADN2530 and TOSA. For additional application information and optical eye diagram performance data, see the EVAL-ADN2530 application note and reference design.

Table 6.

Component	Value	Description
R1, R2	110 Ω	0603 size resistor
R3, R4	300 Ω	0603 size resistor
C3, C4	100 nF	0402 size capacitor, Phycomp 223878719849
L6, L7	160 nH	0603 size inductor, Murata LQW18ANR16
L2, L3		0603 size chip ferrite bead, Murata BLM18HG601
L1, L4, L5, L8	10 µH	0805 size inductor, Murata LQM21FN100M70L

LAYOUT GUIDELINES

Due to the high frequencies at which the ADN2530 operates, take care when designing the PCB layout to obtain optimum performance. Controlled impedance transmission lines must be used for the high speed signal paths. The length of the transmission lines must be kept to a minimum to reduce losses and pattern-dependent jitter. The PCB layout must be symmetrical both on the DATAP and DATAN inputs and on the IMODP and IMODN outputs to ensure a balance between the differential signals. All VCC and GND pins must be connected to solid copper planes by using low inductance connections. When the connections are made through vias, multiple vias can be connected in parallel to reduce the parasitic inductance. Each GND pin must be locally decoupled to VCC with high quality capacitors, see Figure 39. If proper decoupling cannot be achieved using a single capacitor, the user can use multiple capacitors in parallel for each GND pin. A 20 µF tantalum capacitor must be used as the general decoupling capacitor for the entire module. For recommended PCB layouts, including those suitable for XFP modules, contact sales. For guidelines on the surface-mount assembly of the ADN2530, consult the Amkor Technology® "Application Notes for Surface Mount Assembly of Amkor's *Micro*LeadFrame® (MLF®) Packages."

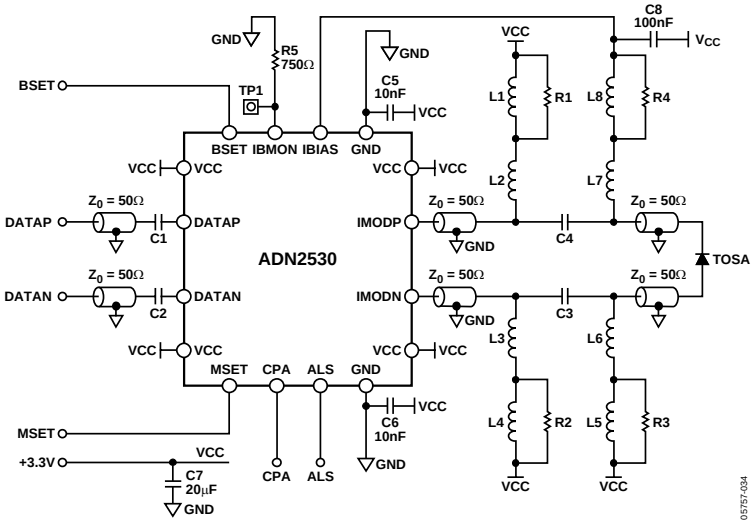

Figure 39. Typical ADN2530 Application Circuit

DESIGN EXAMPLE

This design example covers:

- Headroom calculations for IBIAS, IMODP, and IMODN pins.
- Calculation of the typical voltage required at the BSET and MSET pins to produce the desired bias and modulation currents.
- Calculations of the IBIAS monitor accuracy over the IBIAS current range.

This design example assumes that the impedance of the TOSA is 60 Ω, the forward voltage of the VCSEL at low current is V_F = 1.2 V, IBIAS = 10 mA, IMOD = 10 mA, and VCC = 3.3 V.

Headroom Calculations

To ensure proper device operation, the voltages on the IBIAS, IMODP, and IMODN pins must meet the compliance voltage specifications in Table 1.

Considering the typical application circuit shown in Figure 39, the voltage at the IBIAS pin can be written as

$$V_{IBIAS} = VCC - V_F - (IBIAS \times R_{TOSA}) - V_{LA}$$

where:
VCC is the supply voltage.
V_F is the forward voltage across the laser at low current.
R_{TOSA} is the resistance of the TOSA.
V_{LA} is the dc voltage drop across L5, L6, L7, and L8.

For proper operation, the minimum voltage at the IBIAS pin must be greater than 0.55 V, as specified by the minimum IBIAS compliance specification in Table 1.

Assuming that the voltage drop across the 50 Ω transmission lines is negligible and that V_{LA} = 0 V, V_F = 1.2 V, and IBIAS = 10 mA,

$$V_{IBIAS} = 3.3 - 1.2 - (0.01 \times 60) = 1.5 \text{ V}$$

V_{IBIAS} = 1.5 V > 0.55 V, *which satisfies the requirement*

The maximum voltage at the IBIAS pin must be less than the maximum IBIAS compliance specification as described by

$$V_{COMPLIANCE\_MAX} = VCC - 0.75 - 22 \times IBIAS \text{ (A)}$$

For this example,

$$V_{COMPLIANCE\_MAX} = VCC - 0.75 - 22 \times 0.01 = 2.33 \text{ V}$$

V_{IBIAS} = 1.5 V < 2.33 V, *which satisfies the requirement*

To calculate the headroom at the modulation current pins (IMODP and IMODN), the voltage has a dc component equal to VCC due to the ac-coupled configuration and a swing equal to IMOD × 50 Ω, as R_{TOSA} < 100 Ω. For proper operation of the ADN2530, the voltage at each modulation output pin must be within the normal operation region shown in Figure 35.

Assuming the dc voltage drop across L1, L2, L3, and L4 = 0 V and IMOD = 10 mA, the minimum voltage at the modulation output pins is equal to

$$VCC - (IMOD \times 50)/2 = VCC - 0.25$$

$VCC - 0.25 > VCC - 0.7$ V, *which satisfies the requirement*

The maximum voltage at the modulation output pins is equal to

$$VCC + (IMOD \times 50)/2 = VCC + 0.25$$

$VCC + 0.25 < VCC + 0.7$ V, *which satisfies the requirement*

Headroom calculations must be repeated for the minimum and maximum values of the required IBIAS and IMOD ranges to ensure proper device operation over all operating conditions.

BSET and MSET Pin Voltage Calculation

To set the desired bias and modulation currents, the BSET and MSET pins of the ADN2530 must be driven with the appropriate dc voltage. The voltage range required at the BSET pin to generate the required IBIAS range can be calculated using the BSET voltage to IBIAS gain specified in Table 1. Assuming that IBIAS = 10 mA and the typical IBIAS/V_{BSET} ratio of 20 mA/V, the BSET voltage is given by

$$V_{BSET} = \frac{IBIAS\,(\text{mA})}{20\text{ mA/V}} = \frac{10}{20} = 0.5 \text{ V}$$

The BSET voltage range can be calculated using the required IBIAS range and the minimum and maximum BSET voltage to IBIAS gain values specified in Table 1.

The voltage required at the MSET pin to produce the desired modulation current can be calculated using

$$V_{MSET} = \frac{IMOD}{K}$$

where *K* is the *MSET* voltage to *IMOD* ratio.

The value of K depends on the actual resistance of the TOSA and can be obtained from Figure 34. For a TOSA resistance of 60 Ω, the typical value of K = 24 mA/V. Assuming that IMOD = 10 mA and using the preceding equation, the MSET voltage is given by

$$V_{MSET} = \frac{IMOD\,(\text{mA})}{24\text{ mA/V}} = \frac{10}{24} = 0.42 \text{ V}$$

The MSET voltage range can be calculated using the required IMOD range and the minimum and maximum K values. These can be obtained from the minimum and maximum curves in Figure 34.

IBIAS Monitor Accuracy Calculations

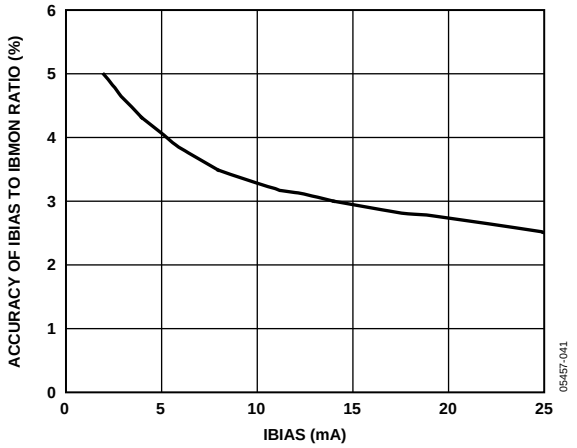

Figure 40. Accuracy of IBIAS to IBMON Ratio

This example assumes that the nominal value of IBIAS is 8 mA and that the IBIAS range for all operating conditions is 4 mA to 14 mA. The accuracy of the IBIAS to IBMON ratio is given in the Table 1 and is plotted in Figure 40.

Referring to Figure 40, the IBMON output current accuracy is ±4.3% for the minimum IBIAS of 4 mA and ±3.0% for the maximum IBIAS value of 14 mA.

The accuracy of the IBMON output current as a percentage of the nominal IBIAS is given by

$$IBMON\_Accuracy_{MIN} = 4\text{ mA}\frac{4.3}{100}\times\frac{100}{8\text{ mA}} = \pm 2.15\%$$

for the minimum IBIAS value, and by

$$IBMON\_Accuracy_{MAX} = 14\text{ mA}\frac{3.0}{100}\times\frac{100}{8\text{ mA}} = \pm 5.25\%$$

for the maximum IBIAS value. This gives a worse-case accuracy for the IBMON output current of ±5.25% of the nominal IBIAS value over all operating conditions. The IBMON output current accuracy numbers can be combined with the accuracy numbers for the 750 Ω IBMON resistor (R_{IBMON}) and any other error sources to calculate an overall accuracy for the IBMON voltage.

OUTLINE DIMENSIONS

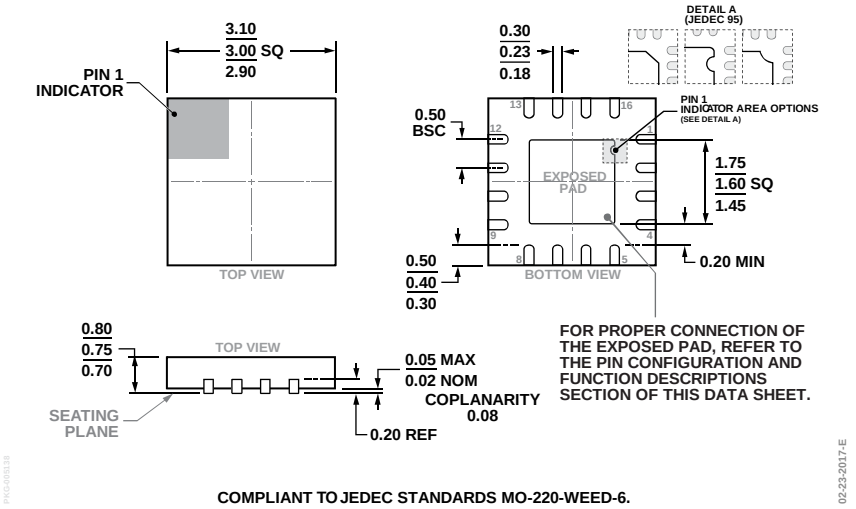

Figure 41. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADN2530YCPZ-500R7	−40°C to +100°C	16-Lead Lead Frame Chip Scale Package [LFCSP], 500 Piece Reel	CP-16-22	F08
ADN2530YCPZ-REEL7	−40°C to +100°C	16-Lead Lead Frame Chip Scale Package [LFCSP], 1500 Piece Reel	CP-16-22	F08

[1] Z = RoHS Compliant Part.