12-Bit, 125 MSPS Dual TxDAC+ Digital-to-Analog Converters

Data Sheet **AD9765**

FEATURES

10-/12-/14-bit dual transmit digital-to-analog converters (DACs)
125 MSPS update rate
Excellent SFDR to Nyquist @ 5 MHz output: 75 dBc
Excellent gain and offset matching: 0.1%
Fully independent or single-resistor gain control
Dual-port or interleaved data
On-chip 1.2 V reference
5 V or 3.3 V operation
Power dissipation: 380 mW @ 5 V
Power-down mode: 50 mW @ 5 V
48-lead LQFP

APPLICATIONS

Communications
Base stations
Digital synthesis
Quadrature modulation
3D ultrasound

GENERAL DESCRIPTION

The AD9763/AD9765/AD9767 are dual-port, high speed, 2-channel, 10-/12-/14-bit CMOS DACs. Each part integrates two high quality TxDAC+® cores, a voltage reference, and digital interface circuitry into a small 48-lead LQFP. The AD9763/AD9765/AD9767 offer exceptional ac and dc performance while supporting update rates of up to 125 MSPS.

The AD9763/AD9765/AD9767 have been optimized for processing I and Q data in communications applications. The digital interface consists of two double-buffered latches as well as control logic. Separate write inputs allow data to be written to the two DAC ports independent of one another. Separate clocks control the update rate of the DACs.

A mode control pin allows the AD9763/AD9765/AD9767 to interface to two separate data ports, or to a single interleaved high speed data port. In interleaving mode, the input data stream is demuxed into its original I and Q data and then latched. The I and Q data is then converted by the two DACs and updated at half the input data rate.

The GAINCTRL pin allows two modes for setting the full-scale current (I_{OUTFS}) of the two DACs. I_{OUTFS} for each DAC can be set independently using two external resistors, or I_{OUTFS} for both DACs can be set by using a single external resistor. See the Gain Control Mode section for important date code information on this feature.

FUNCTIONAL BLOCK DIAGRAM

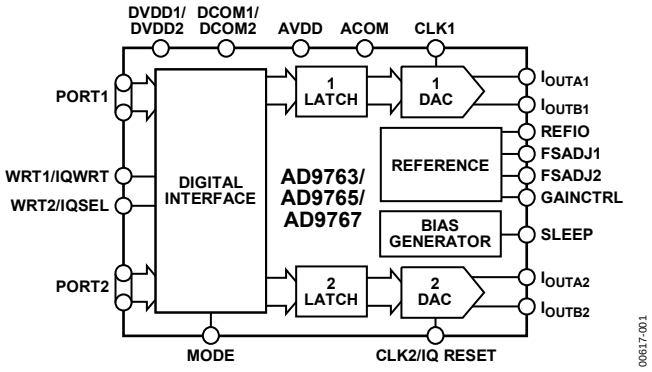

Figure 1.

The DACs utilize a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and maximize dynamic accuracy. Each DAC provides differential current output, thus supporting single-ended or differential applications. Both DACs of the AD9763, AD9765, or AD9767 can be simultaneously updated and can provide a nominal full-scale current of 20 mA. The full-scale currents between each DAC are matched to within 0.1%.

The AD9763/AD9765/AD9767 are manufactured on an advanced, low cost CMOS process. They operate from a single supply of 3.3 V to 5 V and consume 380 mW of power.

PRODUCT HIGHLIGHTS

1. The AD9763/AD9765/AD9767 are members of a pin-compatible family of dual TxDACs providing 8-, 10-, 12-, and 14-bit resolution.
2. Dual 10-/12-/14-Bit, 125 MSPS DACs. A pair of high performance DACs for each part is optimized for low distortion performance and provides flexible transmission of I and Q information.
3. Matching. Gain matching is typically 0.1% of full scale, and offset error is better than 0.02%.
4. Low Power. Complete CMOS dual DAC function operates on 380 mW from a 3.3 V to 5 V single supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low power idle periods.
5. On-Chip Voltage Reference. The AD9763/AD9765/AD9767 each include a 1.20 V temperature-compensated band gap voltage reference.
6. Dual 10-/12-/14-Bit Inputs. The AD9763/AD9765/AD9767 each feature a flexible dual-port interface, allowing dual or interleaved input data.

Rev. G

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6/09—Rev. E to Rev. F

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1/08—Revision E: Initial Combined Version

Revision History: AD9763

1/08—Rev. D to Rev. E

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9/06—Rev. C to Rev. D

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12/99—Rev. 0 to Rev. A

Revision History: AD9765

1/08—Rev. C to Rev. E

9/06—Rev. B to Rev. C

2/00—Rev. A to Rev. B

12/99—Rev. 0 to Rev. A

8/99—Revision 0: Initial Version

Revision History: AD9767

1/08—Rev. C to Rev. E

10/06—Rev. B to Rev. C

2/00—Rev. A to Rev. B

12/99—Rev. 0 to Rev. A

8/99—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V or 5 V, DVDD1 = DVDD2 = 3.3 V or 5 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

	AD9763			AD9765			AD9767			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	10			12			14			Bits
DC ACCURACY[1]										
Integral Linearity Error (INL)	−1	±0.1	+1							LSB
T_A = 25°C				−1.5	±0.4	+1.5	−3.5	±1.5	+3.5	LSB
T_{MIN} to T_{MAX}				−2.0		+2.0	−4.0		+4.0	LSB
Differential Nonlinearity (DNL)										LSB
T_A = 25°C	−0.5	±0.07	+0.5	−0.75	±0.3	+0.75	−2.5	±1.0	+2.5	LSB
T_{MIN} to T_{MAX}				−1.0		+1.0	−3.0		+3.0	LSB
ANALOG OUTPUT										
Offset Error	−0.02		+0.02	−0.02		+0.02	−0.02		+0.02	% of FSR
Gain Error Without Internal Reference	−2	±0.25	+2	−2	±0.25	+2	−2	±0.25	+2	% of FSR
Gain Error with Internal Reference	−5	±1	+5	−5	±1	+5	−5	±1	+5	% of FSR
Gain Match	−1.6	±0.1	+1.6	−1.6	±0.1	+1.6	−1.6	±0.1	+1.6	% of FSR
	−0.14		+0.14	−0.14		+0.14	−0.14		+0.14	dB
Full-Scale Output Current[2]	2.0		20.0	2.0		20.0	2.0		20.0	mA
Output Compliance Range	−1.0		+1.25	−1.0		+1.25	−1.0		+1.25	V
Output Resistance		100			100			100		kΩ
Output Capacitance		5			5			5		pF
REFERENCE OUTPUT										
Reference Voltage	1.14	1.20	1.26	1.14	1.20	1.26	1.14	1.20	1.26	V
Reference Output Current[3]		100			100			100		nA
REFERENCE INPUT										
Input Compliance Range	0.1		1.25	0.1		1.25	0.1		1.25	V
Reference Input Resistance		1			1			1		MΩ
Small-Signal Bandwidth		0.5			0.5			0.5		MHz
TEMPERATURE COEFFICIENTS										
Offset Drift		0			0			0		ppm of FSR/°C
Gain Drift Without Internal Reference		±50			±50			±50		ppm of FSR/°C
Gain Drift with Internal Reference		±100			±100			±100		ppm of FSR/°C
Reference Voltage Drift		±50			±50			±50		ppm/°C
POWER SUPPLY										
Supply Voltages										
AVDD	3	5	5.5	3	5	5.5	3	5	5.5	V
DVDD1, DVDD2	2.7	5	5.5	2.7	5	5.5	2.7	5	5.5	V
Analog Supply Current (I_{AVDD})		71	75		71	75		71	75	mA
Digital Supply Current (I_{DVDD})[4]		5	7		5	7		5	7	mA
Digital Supply Current (I_{DVDD})[5]			15			15			15	mA
Supply Current Sleep Mode (I_{AVDD})		8	12.0		8	12.0		8	12.0	mA
Power Dissipation[4] (5 V, I_{OUTFS} = 20 mA)		380	410		380	410		380	410	mW
Power Dissipation[5] (5 V, I_{OUTFS} = 20 mA)		420	450		420	450		420	450	mW
Power Dissipation[6] (5 V, I_{OUTFS} = 20 mA)		450			450			450		mW
Power Supply Rejection Ratio[7]—AVDD	−0.4		+0.4	−0.4		+0.4	−0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio[7]—DVDD	−0.025		+0.025	−0.025		+0.025	−0.025		+0.025	% of FSR/V
OPERATING RANGE	−40		+85	−40		+85	−40		+85	°C

[1] Measured at I_{OUTA}, driving a virtual ground.
[2] Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.
[3] An external buffer amplifier with input bias current <100 nA should be used to drive any external load.
[4] Measured at f_{CLK} = 25 MSPS and f_{OUT} = 1.0 MHz.
[5] Measured at f_{CLK} = 100 MSPS and f_{OUT} = 1 MHz.
[6] Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and R_{LOAD} = 50 Ω at I_{OUTA} and I_{OUTB}, f_{CLK} = 100 MSPS, and f_{OUT} = 40 MHz.
[7] ±10% power supply variation.

DYNAMIC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V or 5 V, DVDD1 = DVDD2 = 3.3 V or 5 V, I_{OUTFS} = 20 mA, differential transformer-coupled output, 50 Ω doubly terminated, unless otherwise noted.

Table 2.

	AD9763			AD9765			AD9767			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE										
Maximum Output Update Rate (f_{CLK})	125			125			125			MSPS
Output Settling Time (t_{ST}) to 0.1%[1]		35			35			35		ns
Output Propagation Delay (t_{PD})		1			1			1		ns
Glitch Impulse		5			5			5		pV-s
Output Rise Time (10% to 90%)[1]		2.5			2.5			2.5		ns
Output Fall Time (90% to 10%)[1]		2.5			2.5			2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50			50			50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30			30			30		pA/√Hz
AC LINEARITY										
Spurious-Free Dynamic Range to Nyquist										
f_{CLK} = 100 MSPS, f_{OUT} = 1.00 MHz										
0 dBFS Output	69	78		70	81		71	82		dBc
–6 dBFS Output		74			77			77		dBc
–12 dBFS Output		69			72			73		dBc
–18 dBFS Output		61			70			70		dBc
f_{CLK} = 65 MSPS, f_{OUT} = 1.00 MHz		79			81			82		dBc
f_{CLK} = 65 MSPS, f_{OUT} = 2.51 MHz		78			79			80		dBc
f_{CLK} = 65 MSPS, f_{OUT} = 5.02 MHz		75			78			79		dBc
f_{CLK} = 65 MSPS, f_{OUT} = 14.02 MHz		66			68			70		dBc
f_{CLK} = 65 MSPS, f_{OUT} = 25 MHz		55			55			55		dBc
f_{CLK} = 125 MSPS, f_{OUT} = 25 MHz		67			67			67		dBc
f_{CLK} = 125 MSPS, f_{OUT} = 40 MHz		60			60			70		dBc
Spurious-Free Dynamic Range Within a Window										
f_{CLK} = 100 MSPS, f_{OUT} = 1.00 MHz; 2 MHz Span	78	85		80	90		82	91		dBc
f_{CLK} = 50 MSPS, f_{OUT} = 5.02 MHz; 10 MHz Span		80			88			88		dBc
f_{CLK} = 65 MSPS, f_{OUT} = 5.03 MHz; 10 MHz Span		82			88			88		dBc
f_{CLK} = 125 MSPS, f_{OUT} = 5.04 MHz; 10 MHz Span		82			88			88		dBc
Total Harmonic Distortion										
f_{CLK} = 100 MSPS, f_{OUT} = 1.00 MHz		–77	–69		–80	–70		–81	–71	dBc
f_{CLK} = 50 MSPS, f_{OUT} = 2.00 MHz		–77			–78			–79		dBc
f_{CLK} = 125 MSPS, f_{OUT} = 4.00 MHz		–74			–75			–83		dBc
f_{CLK} = 125 MSPS, f_{OUT} = 10.00 MHz		–72			–75			–80		dBc
Multitone Power Ratio (Eight Tones at 110 kHz Spacing)										
f_{CLK} = 65 MSPS, f_{OUT} = 2.00 MHz to 2.99 MHz										
0 dBFS Output		76			80			80		dBc
–6 dBFS Output		74			79			79		dBc
–12 dBFS Output		71			77			78		dBc
–18 dBFS Output		67			75			76		dBc
Channel Isolation										
f_{CLK} = 125 MSPS, f_{OUT} = 10 MHz		85			85			85		dBc
f_{CLK} = 125 MSPS, f_{OUT} = 40 MHz		77			77			77		dBc

[1] Measured single-ended into 50 Ω load.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V or 5 V, DVDD1 = DVDD2 = 3.3 V or 5 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic 1 Voltage @ DVDD1 = DVDD2 = 5 V	3.5	5		V
Logic 1 Voltage @ DVDD1 = DVDD2 = 3.3 V	2.1	3		V
Logic 0 Voltage @ DVDD1 = DVDD2 = 5 V		0	1.3	V
Logic 0 Voltage @ DVDD1 = DVDD2 = 3.3 V	0		0.9	V
Logic 1 Current	−10		+10	µA
Logic 0 Current	−10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulse Width (t_{LPW}, t_{CPW})	3.5			ns

Timing Diagram

See Table 3 and the DAC Timing section for more information about the timing specifications.

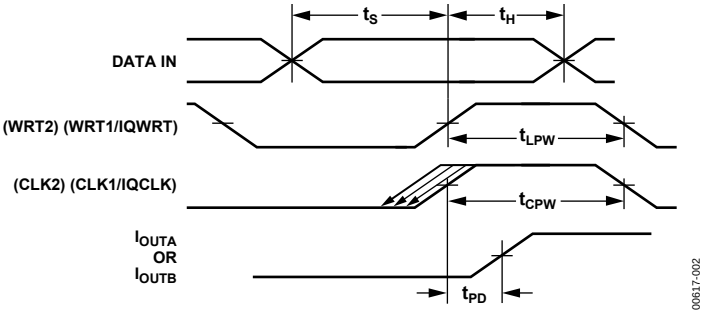


Figure 2. Timing Diagram for Dual and Interleaved Modes

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect To	Rating
AVDD	ACOM	−0.3 V to +6.5 V
DVDD1, DVDD2	DCOM1/DCOM2	−0.3 V to +6.5 V
ACOM	DCOM1/DCOM2	−0.3 V to +0.3 V
AVDD	DVDD1/DVDD2	−6.5 V to +6.5 V
MODE, CLK1/IQCLK, CLK2/IQRESET, WRT1/IQWRT, WRT2/IQSEL	DCOM1/DCOM2	−0.3 V to DVDD1/ DVDD2 + 0.3 V
Digital Inputs	DCOM1/DCOM2	−0.3 V to DVDD1/ DVDD2 + 0.3 V
I_{OUTA1}/I_{OUTA2}, I_{OUTB1}/I_{OUTB2}	ACOM	−1.0 V to AVDD + 0.3 V
REFIO, FSADJ1, FSADJ2	ACOM	−0.3 V to AVDD + 0.3 V
GAINCTRL, SLEEP	ACOM	−0.3 V to AVDD + 0.3 V
Junction Temperature		150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
48-Lead LQFP	91	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

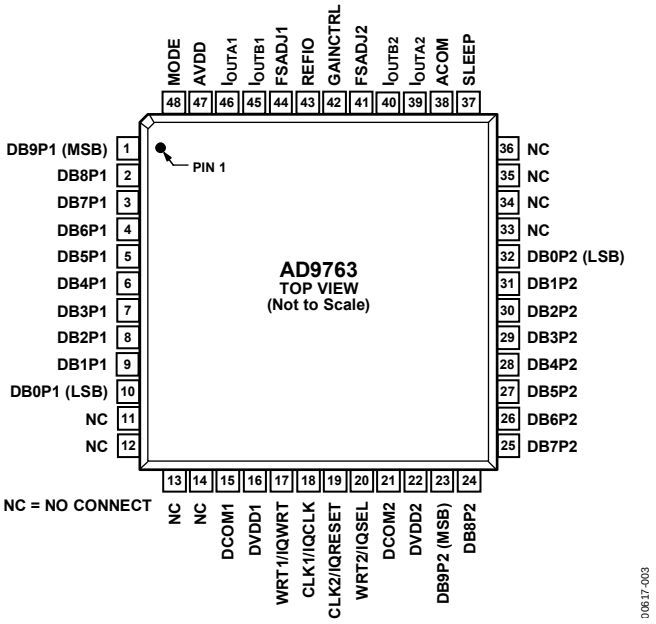


Figure 3. AD9763 Pin Configuration

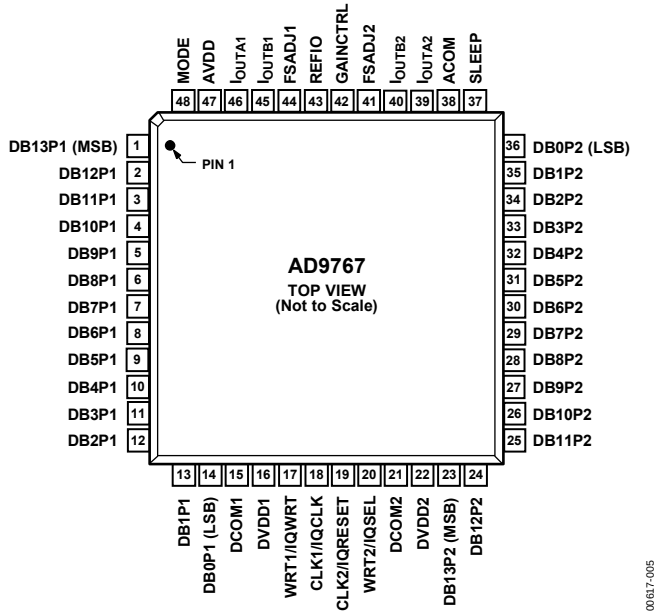


Figure 5. AD9767 Pin Configuration

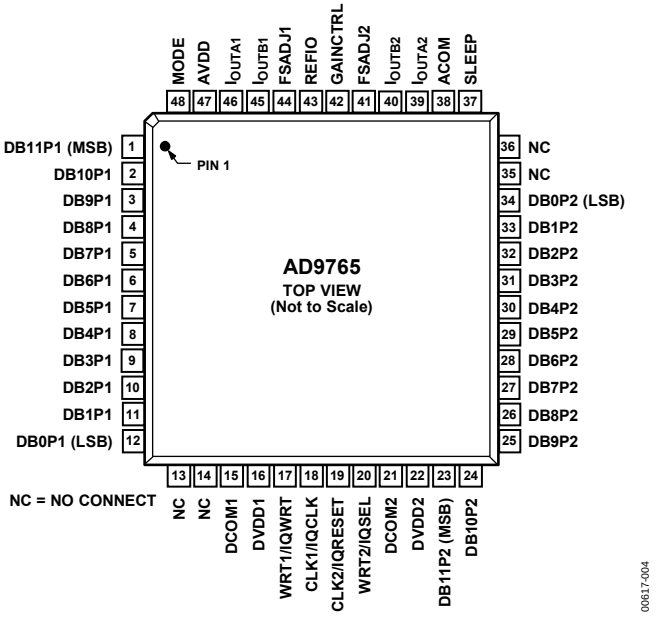


Figure 4. AD9765 Pin Configuration

Table 6. Pin Function Descriptions

Pin No.				
AD9763	**AD9765**	**AD9767**	**Mnemonic**	**Description**
1 to 10	1 to 12	1 to 14	DBxP1	Data Bit Pins (Port 1)
11 to 14, 33 to 36	13, 14, 35, 36	N/A	NC	No Connect
15, 21	15, 21	15, 21	DCOM1, DCOM2	Digital Common
16, 22	16, 22	16, 22	DVDD1, DVDD2	Digital Supply Voltage
17	17	17	WRT1/IQWRT	Input Write Signal for PORT 1 (IQWRT in Interleaving Mode)
18	18	18	CLK1/IQCLK	Clock Input for DAC1 (IQCLK in Interleaving Mode)
19	19	19	CLK2/IQRESET	Clock Input for DAC2 (IQRESET in Interleaving Mode)
20	20	20	WRT2/IQSEL	Input Write Signal for PORT 2 (IQSEL in Interleaving Mode)
23 to 32	23 to 34	23 to 36	DBxP2	Data Bit Pins (Port 2)
37	37	37	SLEEP	Power-Down Control Input
38	38	38	ACOM	Analog Common
39, 40	39, 40	39, 40	I_{OUTA2}, I_{OUTB2}	Port 2 Differential DAC Current Outputs
41	41	41	FSADJ2	Full-Scale Current Output Adjust for DAC2
42	42	42	GAINCTRL	Master/Slave Resistor Control Mode
43	43	43	REFIO	Reference Input/Output
44	44	44	FSADJ1	Full-Scale Current Output Adjust for DAC1
45, 46	45, 46	45, 46	I_{OUTB1}, I_{OUTA1}	Port 1 Differential DAC Current Outputs
47	47	47	AVDD	Analog Supply Voltage
48	48	48	MODE	Mode Select (1 = dual port, 0 = interleaved)

TYPICAL PERFORMANCE CHARACTERISTICS

AD9763

AVDD = 3.3 V or 5 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, 50 Ω doubly terminated load, differential output, T_A = 25°C, SFDR up to Nyquist, unless otherwise noted.

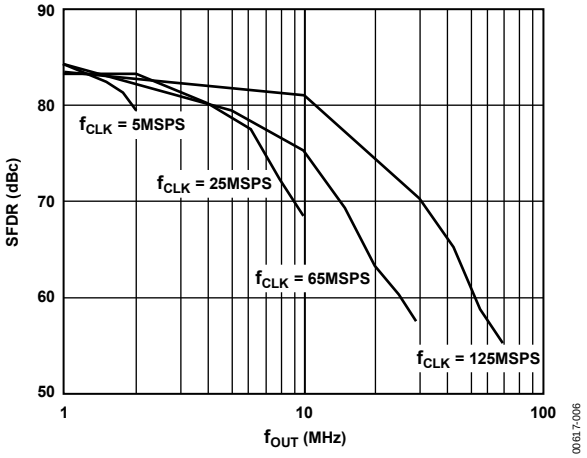


Figure 6. SFDR vs. f_{OUT} @ 0 dBFS

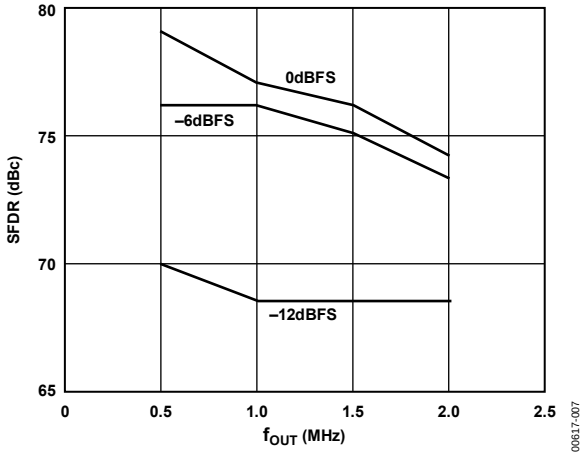


Figure 7. SFDR vs. f_{OUT} @ 5 MSPS

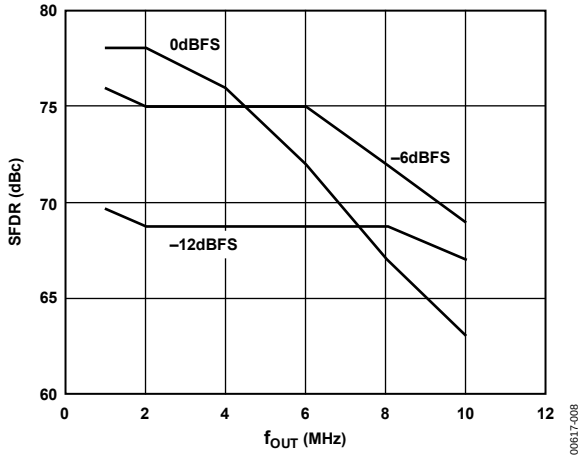


Figure 8. SFDR vs. f_{OUT} @ 25 MSPS

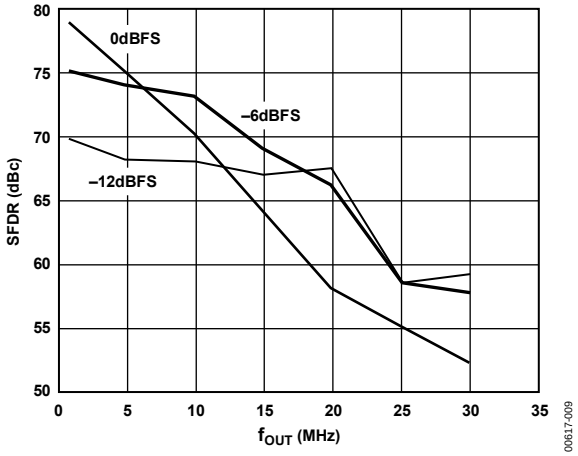


Figure 9. SFDR vs. f_{OUT} @ 65 MSPS

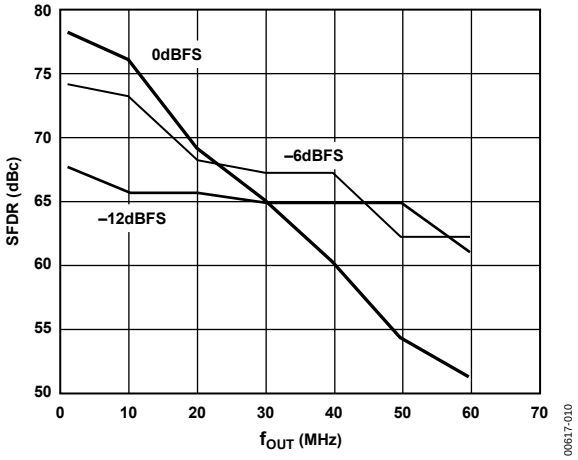


Figure 10. SFDR vs. f_{OUT} @ 125 MSPS

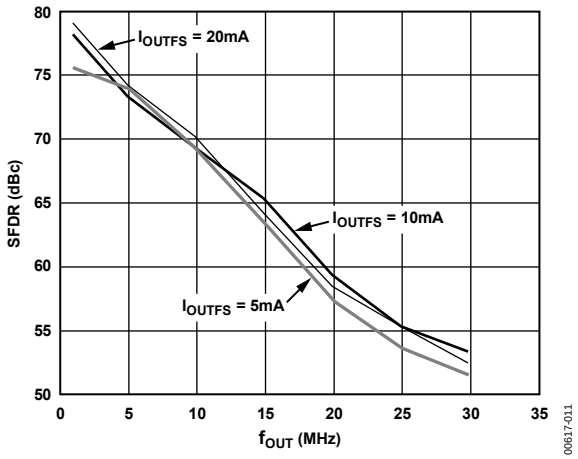


Figure 11. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS and 0 dBFS

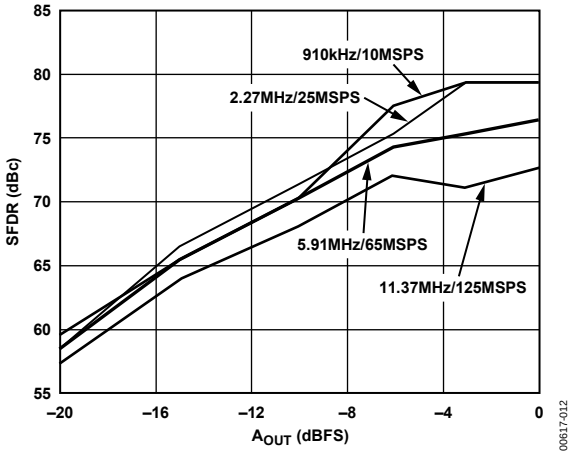


Figure 12. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/11$

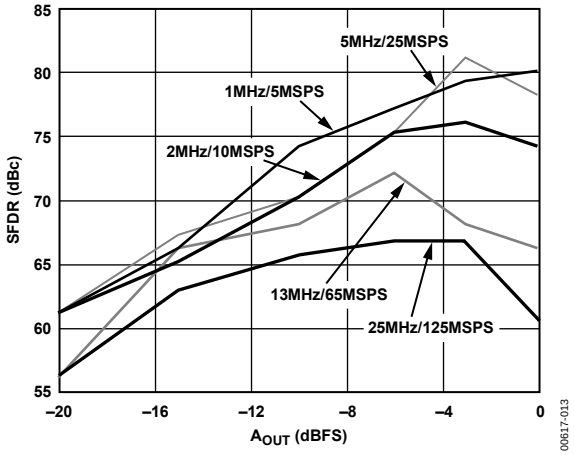


Figure 13. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/5$

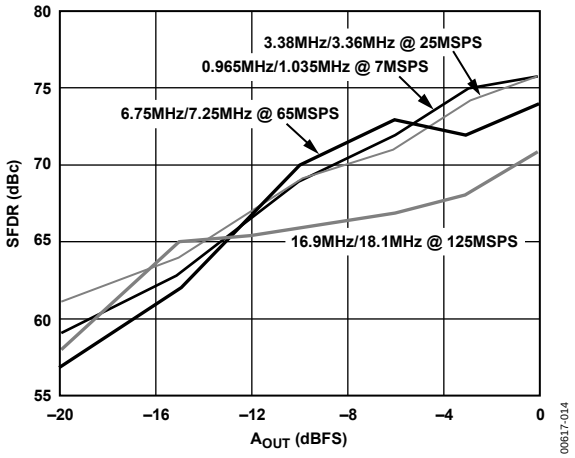


Figure 14. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/7$

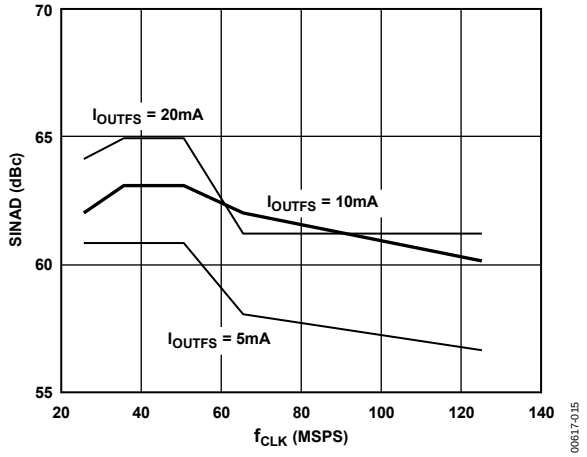


Figure 15. SINAD vs. f_{CLK} and I_{OUTFS} @ f_{OUT} = 5 MHz and 0 dBFS

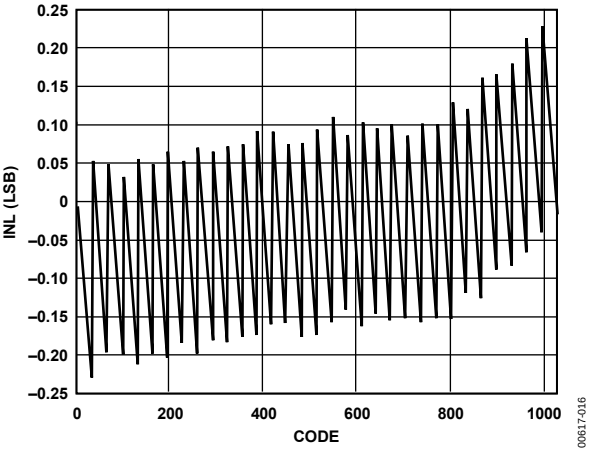


Figure 16. Typical INL

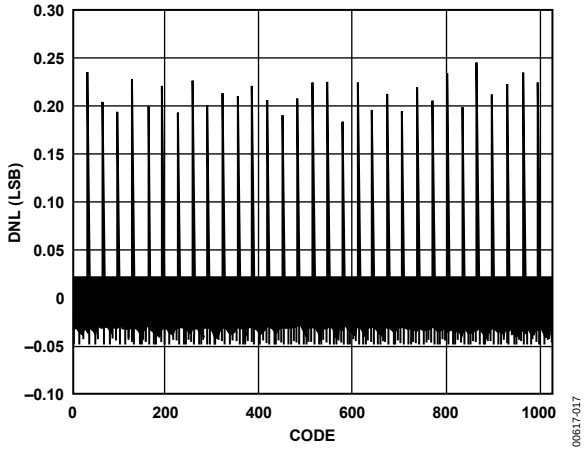


Figure 17. Typical DNL

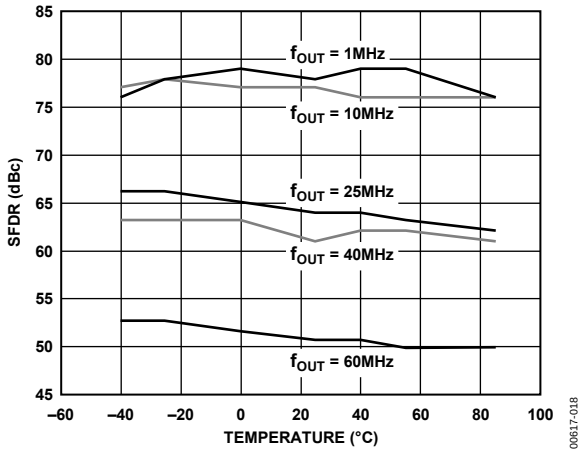


Figure 18. SFDR vs. Temperature @ f_{CLK} = 125 MSPS, 0 dBFS

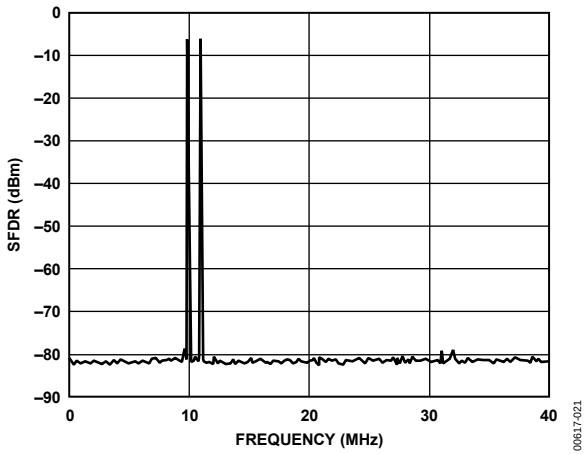


Figure 21. Dual-Tone SFDR @ f_{CLK} = 125 MSPS

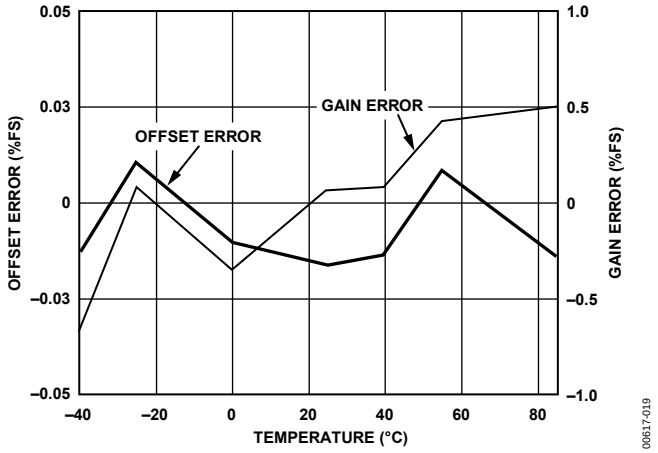


Figure 19. Gain and Offset Error vs. Temperature @ f_{CLK} = 125 MSPS

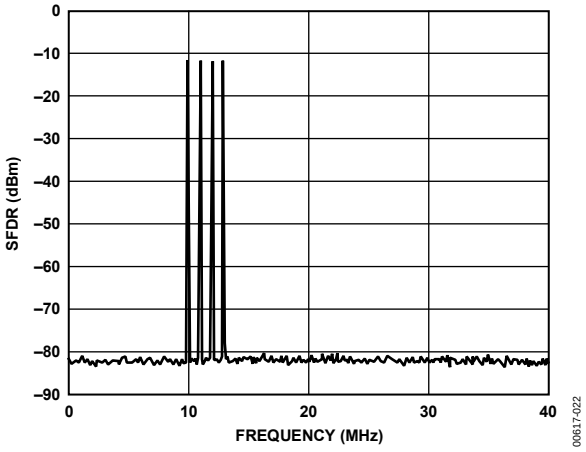


Figure 22. Four-Tone SFDR @ f_{CLK} = 125 MSPS

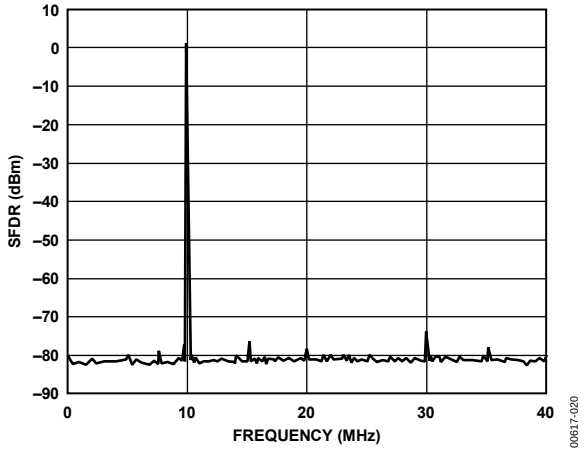


Figure 20. Single-Tone SFDR @ f_{CLK} = 125 MSPS

AD9765

AVDD = 3.3 V or 5 V, DVDD = 3.3 V or 5 V, I_{OUTFS} = 20 mA, 50 Ω doubly terminated load, differential output, T_A = 25°C, SFDR up to Nyquist, unless otherwise noted.

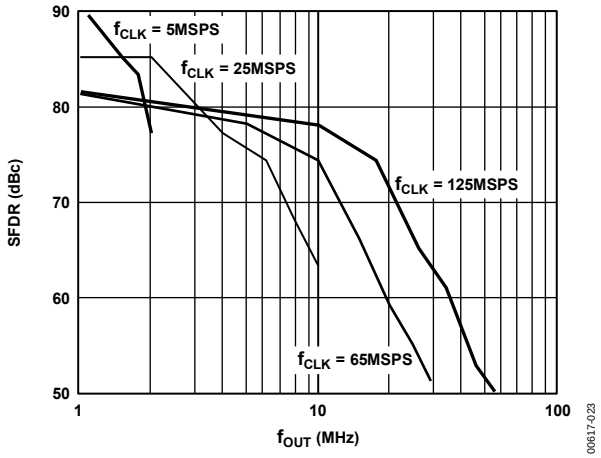


Figure 23. SFDR vs. f_{OUT} @ 0 dBFS

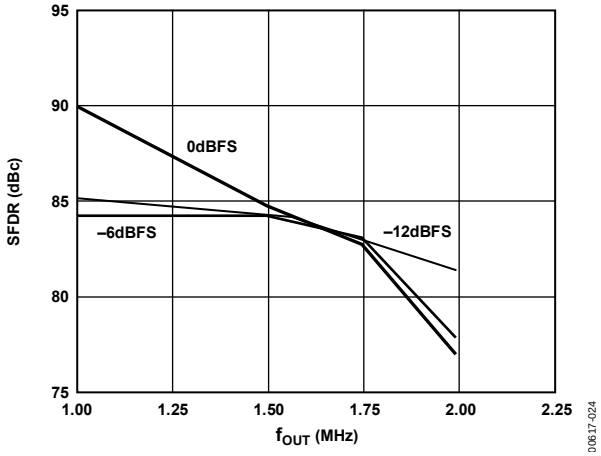


Figure 24. SFDR vs. f_{OUT} @ 5 MSPS

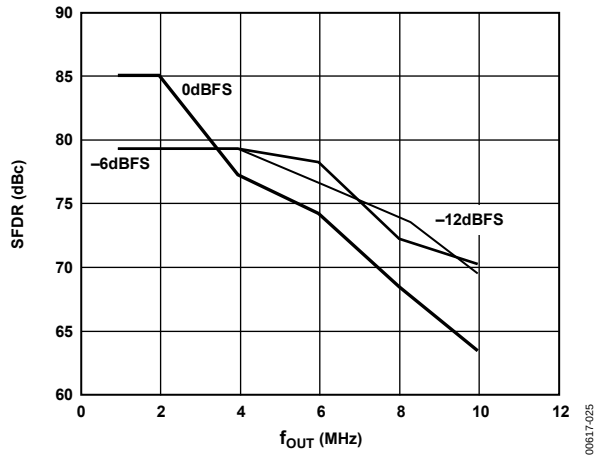


Figure 25. SFDR vs. f_{OUT} @ 25 MSPS

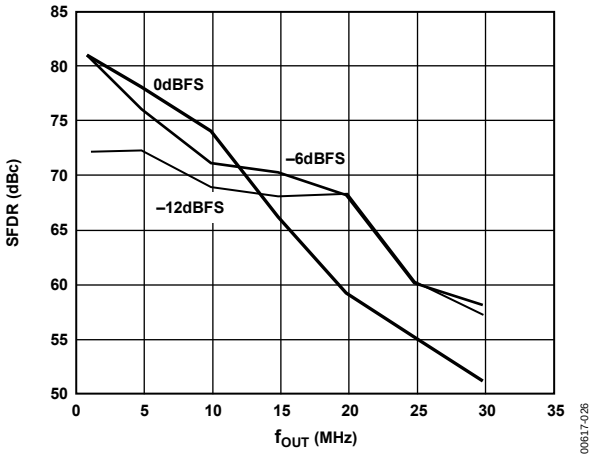


Figure 26. SFDR vs. f_{OUT} @ 65 MSPS

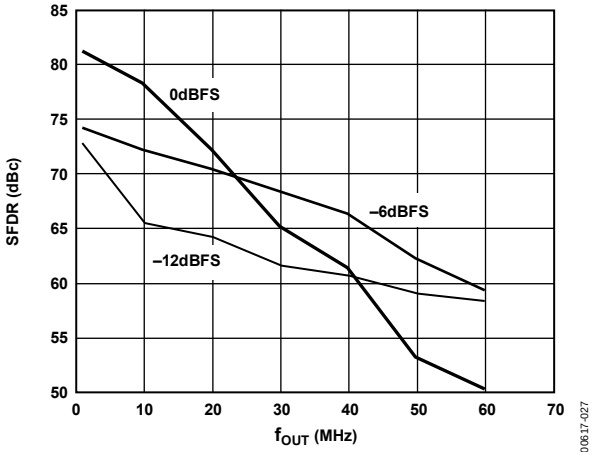


Figure 27. SFDR vs. f_{OUT} @ 125 MSPS

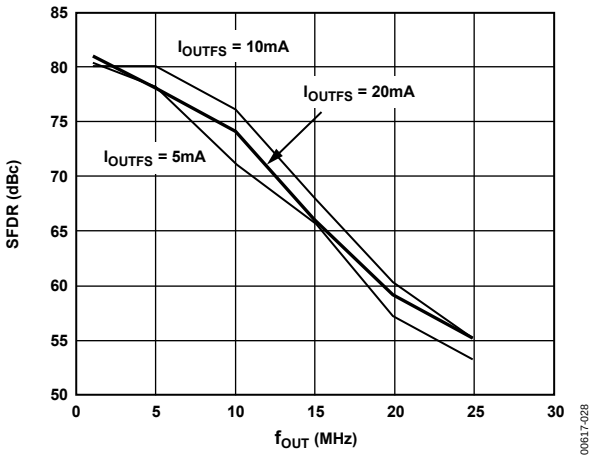


Figure 28. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS and 0 dBFS

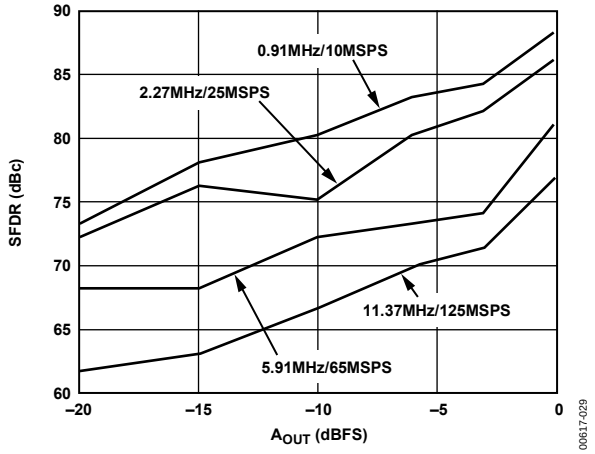


Figure 29. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/11$

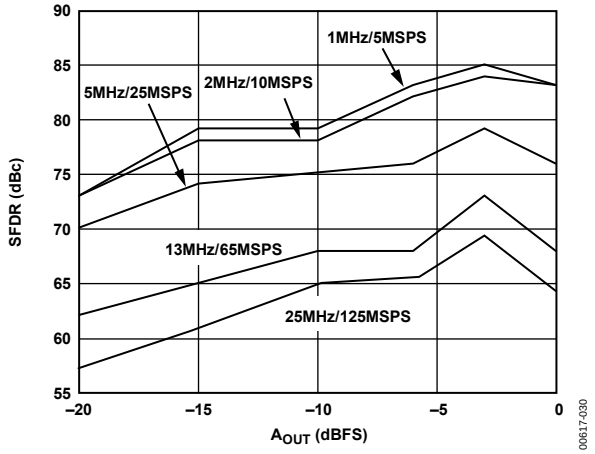


Figure 30. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/5$

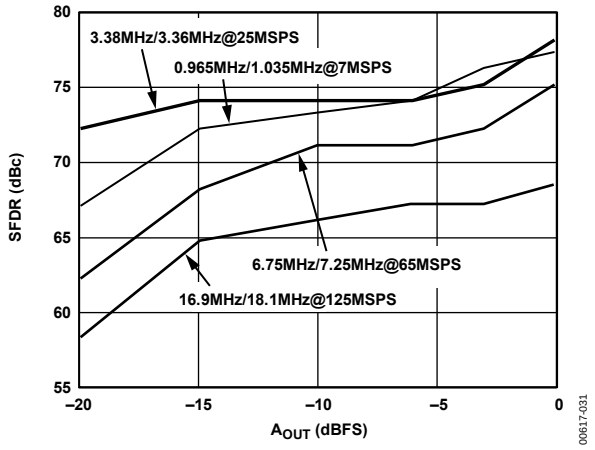


Figure 31. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/7$

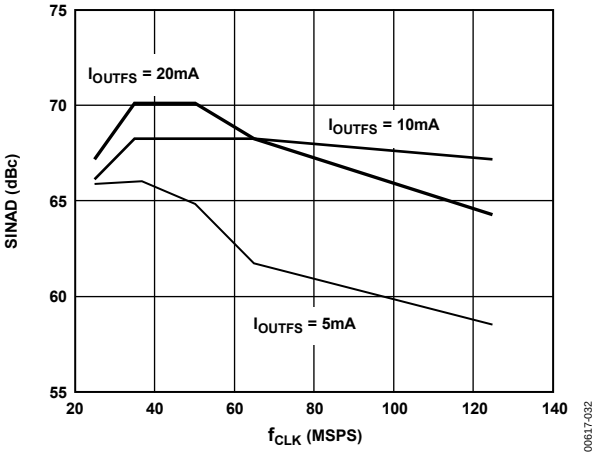


Figure 32. SINAD vs. f_{CLK} and I_{OUTFS} @ f_{OUT} = 5 MHz and 0 dBFS

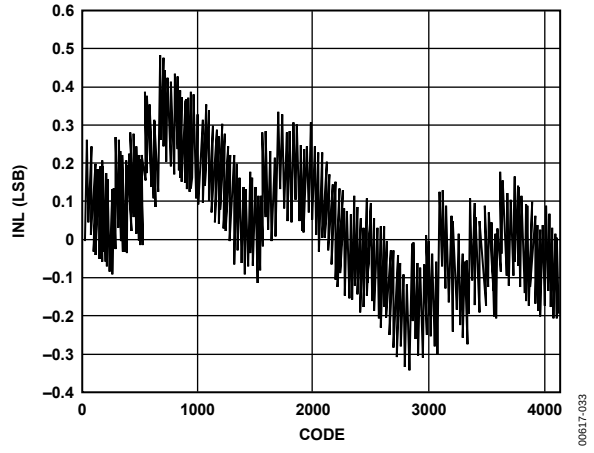


Figure 33. Typical INL

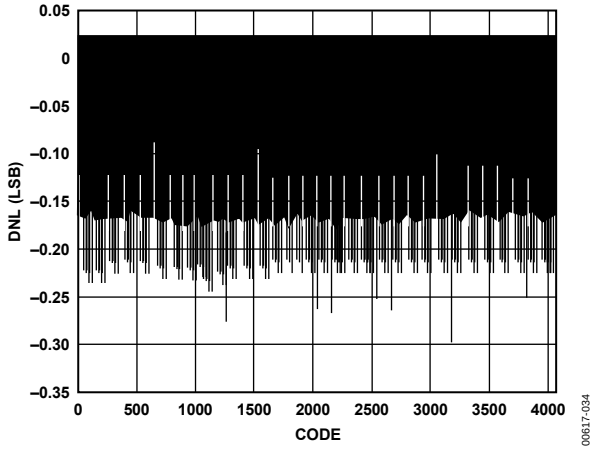


Figure 34. Typical DNL

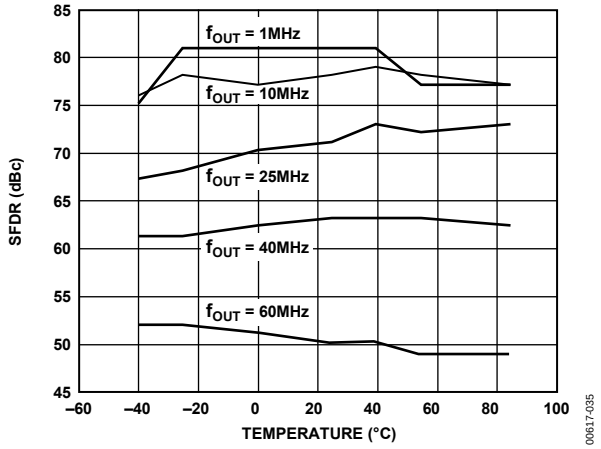


Figure 35. SFDR vs. Temperature @ 125 MSPS, 0 dBFS

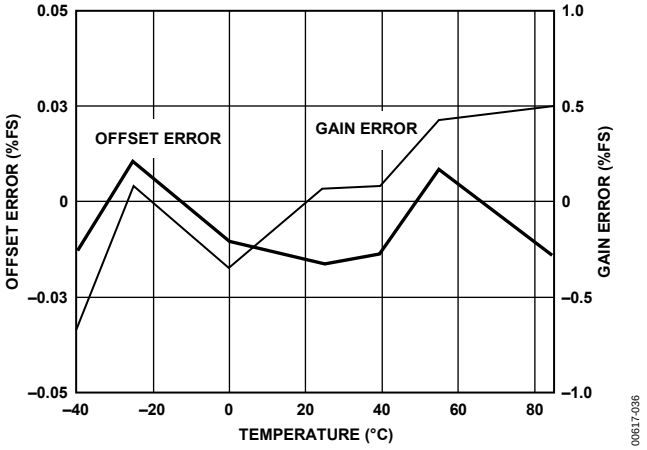


Figure 36. Gain and Offset Error vs. Temperature @ f_{CLK} = 125 MSPS

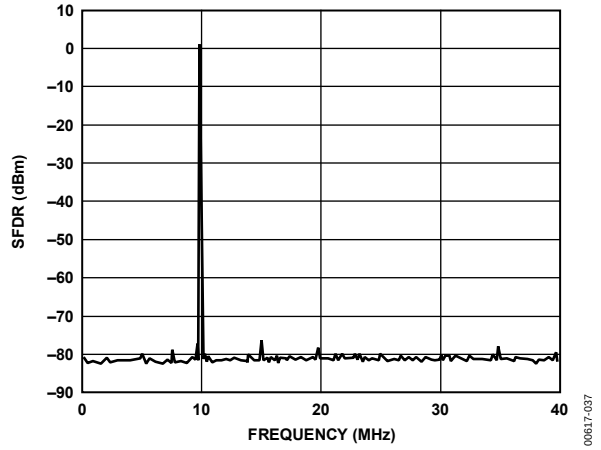


Figure 37. Single-Tone SFDR @ f_{CLK} = 125 MSPS

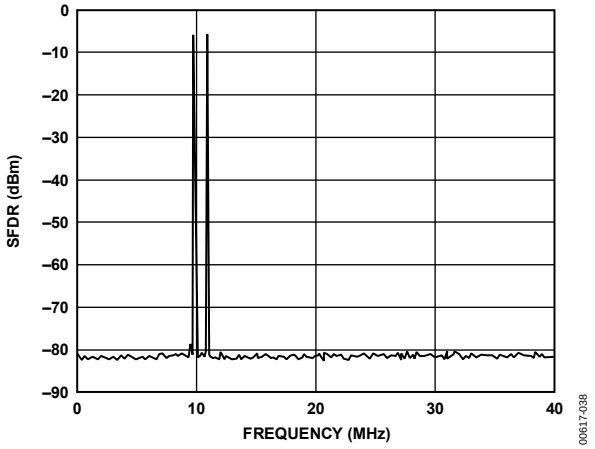


Figure 38. Dual-Tone SFDR @ f_{CLK} = 125 MSPS

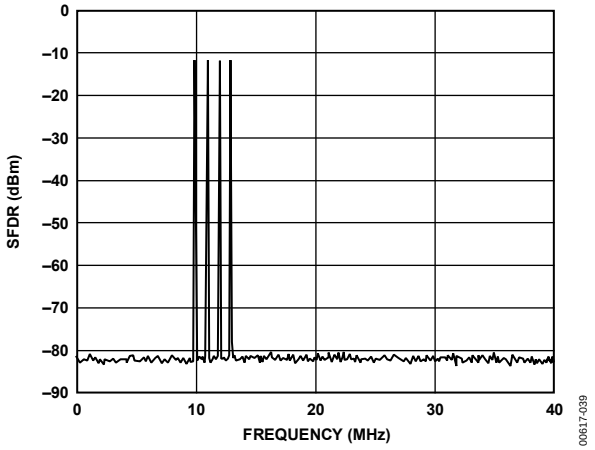


Figure 39. Four-Tone SFDR @ f_{CLK} = 125 MSPS

AD9767

AVDD = 3.3 V or 5 V, DVDD = 3.3 V or 5 V, I_{OUTFS} = 20 mA, 50 Ω doubly terminated load, differential output, T_A = 25°C, SFDR up to Nyquist, unless otherwise noted.

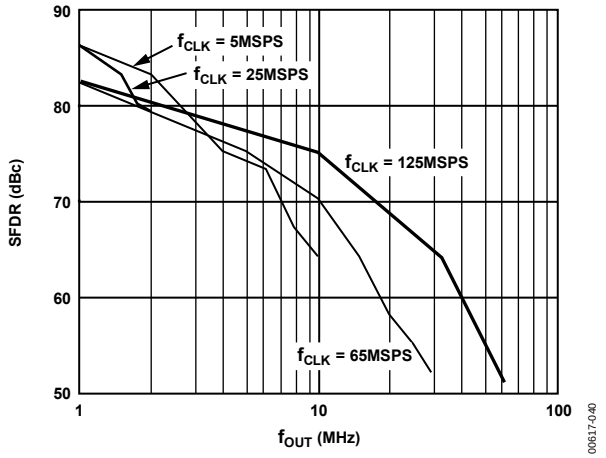


Figure 40. SFDR vs. f_{OUT} @ 0 dBFS

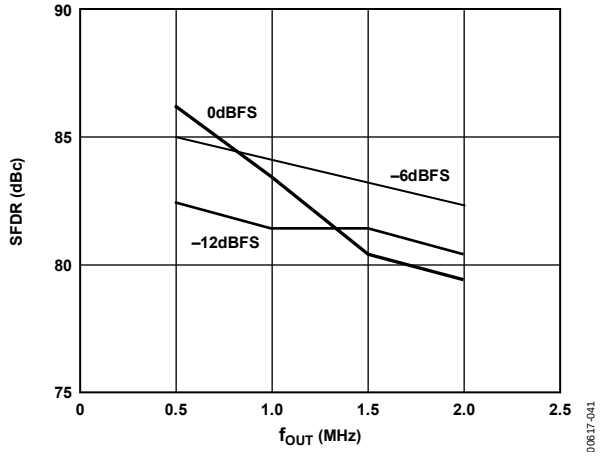


Figure 41. SFDR vs. f_{OUT} @ 5 MSPS

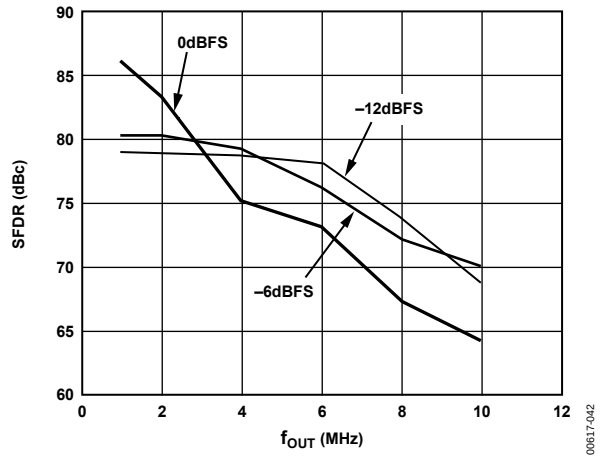


Figure 42. SFDR vs. f_{OUT} @ 25 MSPS

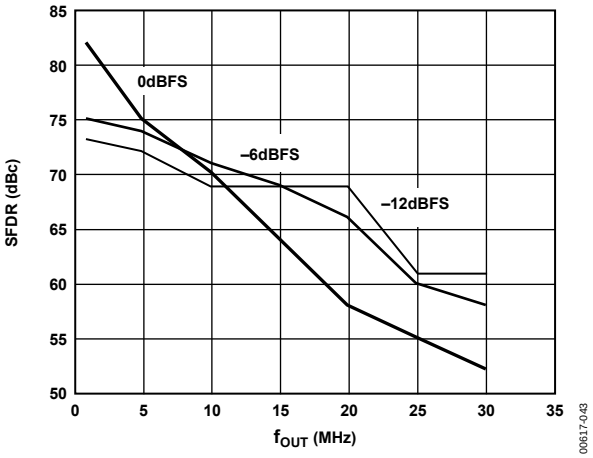


Figure 43. SFDR vs. f_{OUT} @ 65 MSPS

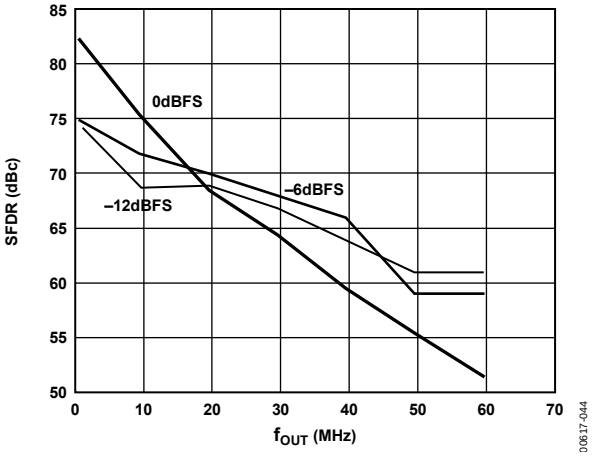


Figure 44. SFDR vs. f_{OUT} @ 125 MSPS

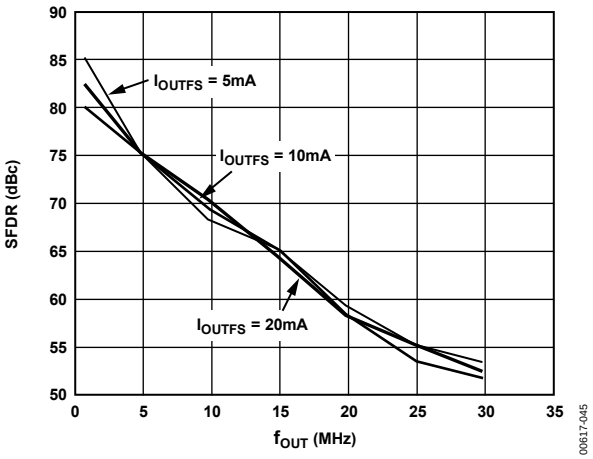


Figure 45. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS and 0 dBFS

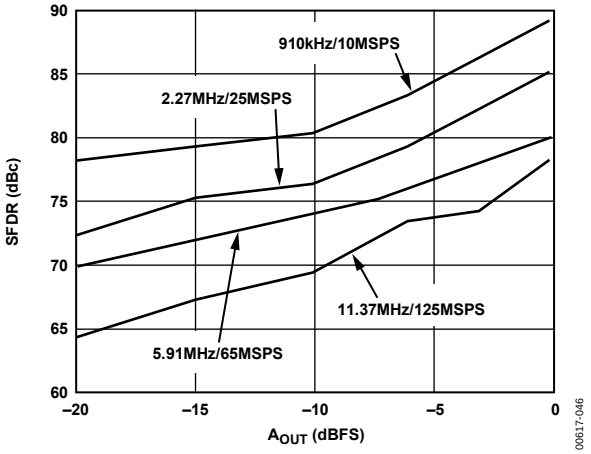


Figure 46. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/11$

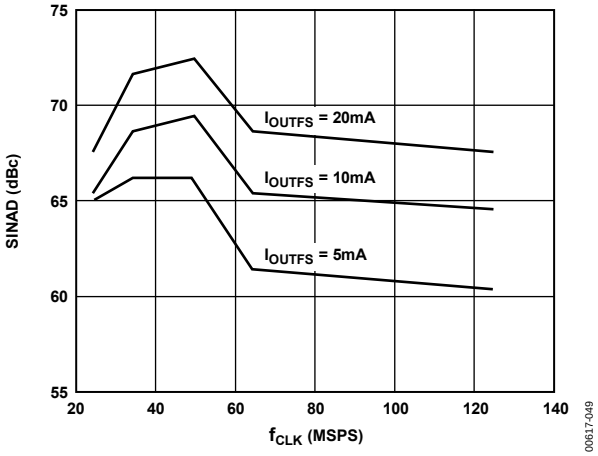


Figure 49. SINAD vs. f_{CLK} and I_{OUTFS} @ f_{OUT} = 5 MHz and 0 dBFS

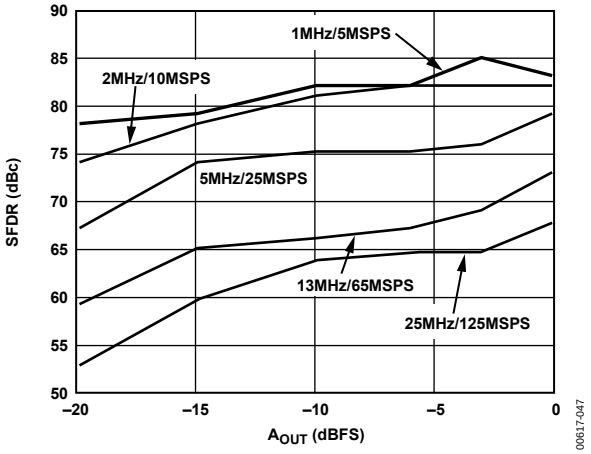


Figure 47. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/5$

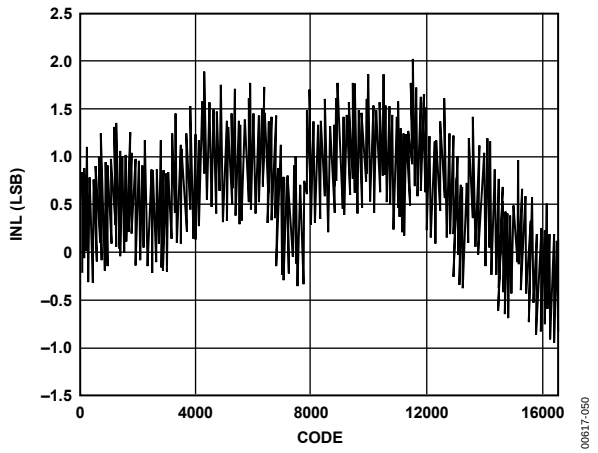


Figure 50. Typical INL

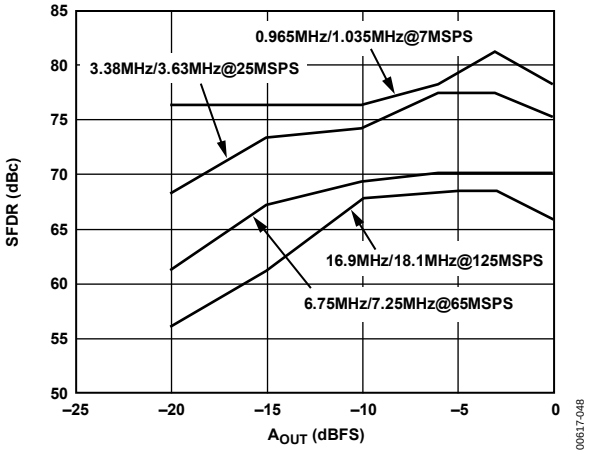


Figure 48. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/7$

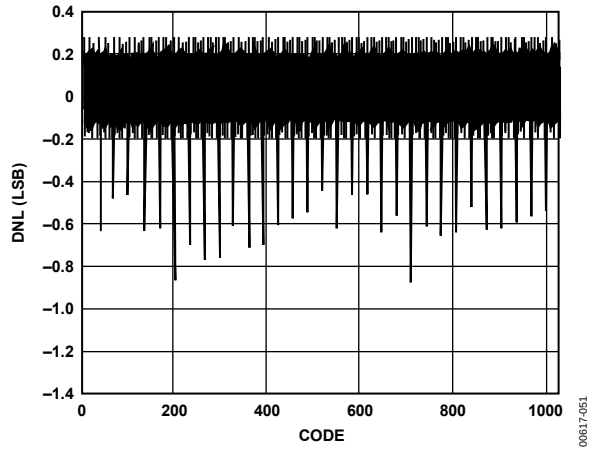


Figure 51. Typical DNL

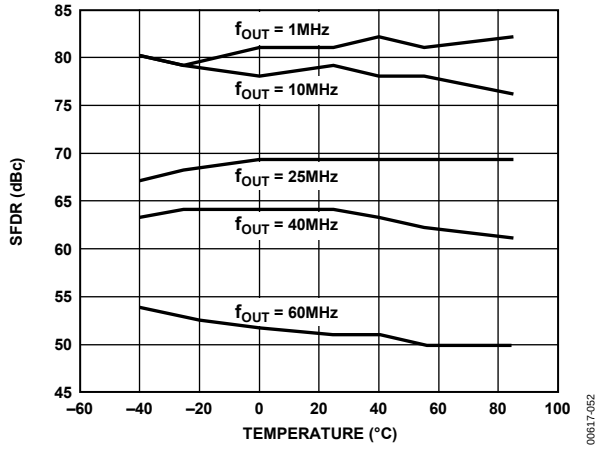


Figure 52. SFDR vs. Temperature @ 125 MSPS, 0 dBFS

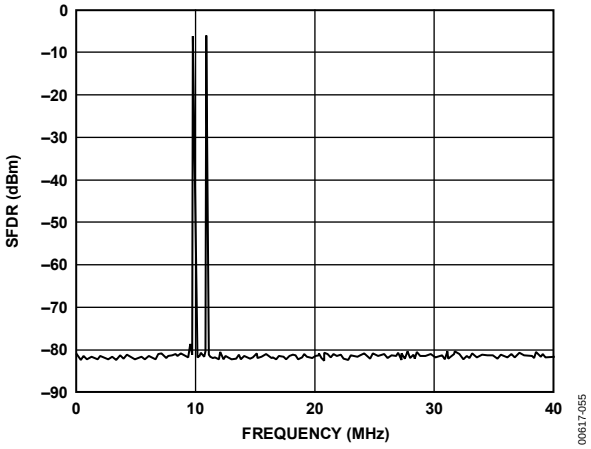


Figure 55. Dual-Tone SFDR @ f_{CLK} = 125 MSPS

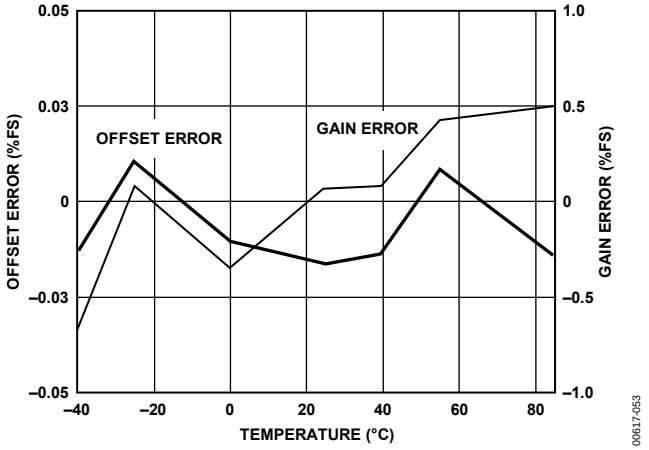


Figure 53. Gain and Offset Error vs. Temperature @ f_{CLK} = 125 MSPS

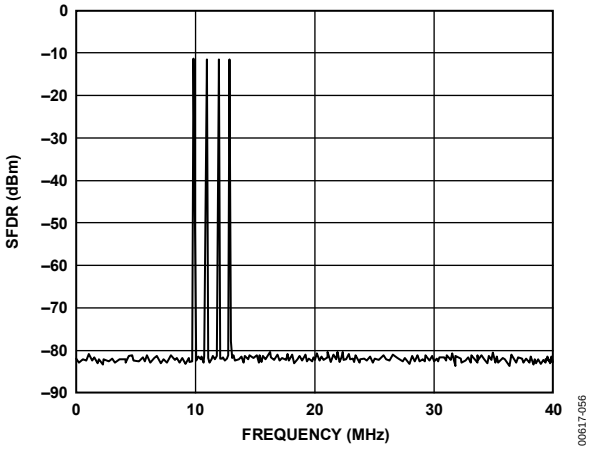


Figure 56. Four-Tone SFDR @ f_{CLK} = 125 MSPS

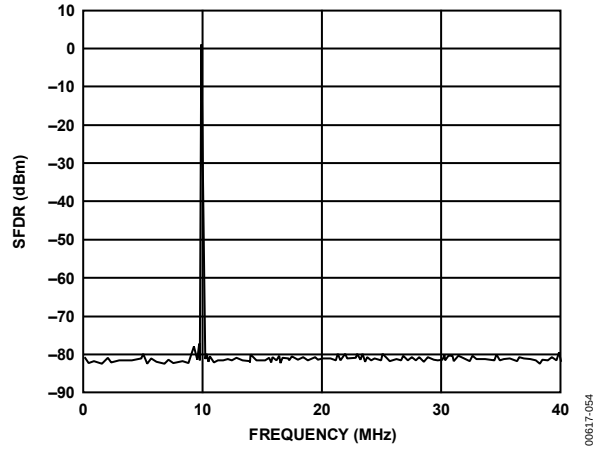


Figure 54. Single-Tone SFDR @ f_{CLK} = 125 MSPS

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of zero. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
Gain error is the difference between the actual and ideal output spans. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in part per million (ppm) of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius (ppm/°C).

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in picovolts per second (pV-s).

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

THEORY OF OPERATION

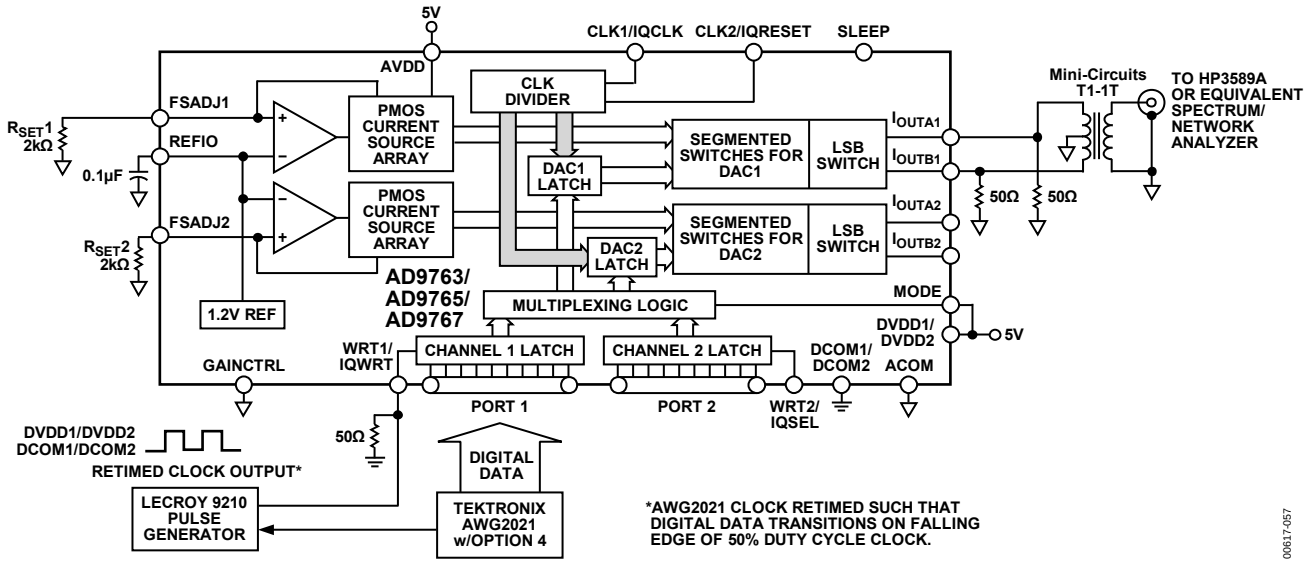
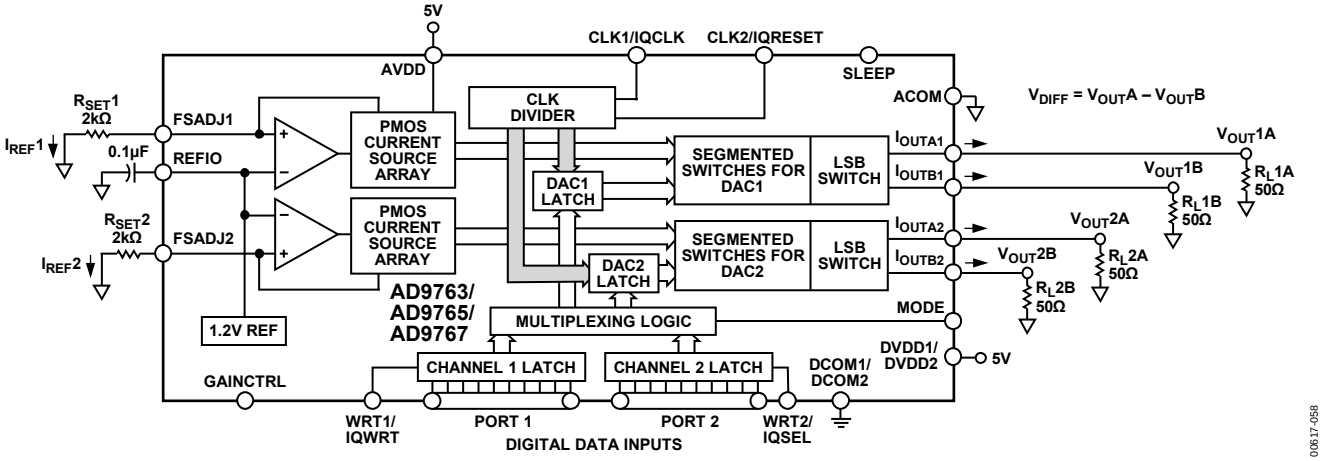


Figure 57. Basic AC Characterization Test Setup for AD9763/AD9765/AD9767, Testing Port 1 in Dual-Port Mode, Using Independent GAINCTRL Resistors on FSADJ1 and FSADJ2



NOTES
1. IN THIS CONFIGURATION, THE 22nF CAPACITOR AND 256Ω RESISTOR ARE NOT REQUIRED BECAUSE R_{SET} = 2kΩ.

Figure 58. Simplified Block Diagram

FUNCTIONAL DESCRIPTION

Figure 58 shows a simplified block diagram of the AD9763/AD9765/AD9767. The AD9763/AD9765/AD9767 consist of two DACs, each one with its own independent digital control logic and full-scale output current control. Each DAC contains a PMOS current source array capable of providing up to 20 mA of full-scale current (I_{OUTFS}).

The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSB is a binary weighted fraction of the middle bit current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances the dynamic performance for multitone or low amplitude signals and helps maintain the high output impedance of each DAC (that is, >100 kΩ).

All of these current sources are switched to one of the two output nodes (that is, I_{OUTA} or I_{OUTB}) via the PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9763/AD9765/AD9767 have separate power supply inputs (that is, AVDD and DVDD1/DVDD2) that can operate independently at 3.3 V or 5 V. The digital section, which is capable of operating up to a 125 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V band gap voltage reference, and two reference control amplifiers.

The full-scale output current of each DAC is regulated by separate reference control amplifiers and can be set from 2 mA to 20 mA via an external network connected to the full scale adjust (FSADJ) pin. The external network, in combination with both the reference control amplifier and voltage reference (V_{REFIO}) sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current (I_{OUTFS}) is 32 × I_{REF}.

REFERENCE OPERATION

The AD9763/AD9765/AD9767 contain an internal 1.20 V band gap reference. This can easily be overridden by a low noise external reference with no effect on performance. REFIO serves as either an input or output, depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1 µF capacitor. The internal reference voltage is present at REFIO. If the voltage at REFIO is used elsewhere in the circuit, an external buffer amplifier with an input bias current of less than 100 nA should be used. An example of the use of the internal reference is shown in Figure 59.

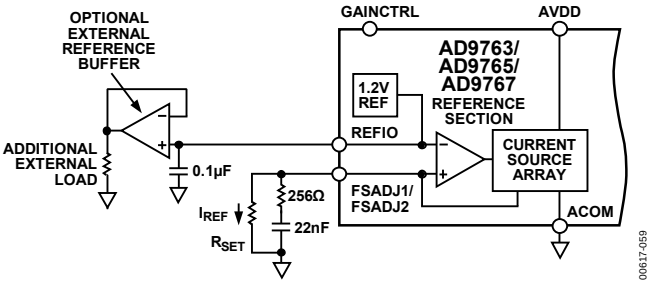


Figure 59. Internal Reference Configuration

An external reference can be applied to REFIO as shown in Figure 60. The external reference can provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. The 0.1 µF compensation capacitor is not required because the internal reference is overridden and the relatively high input impedance of REFIO minimizes any loading of the external reference.

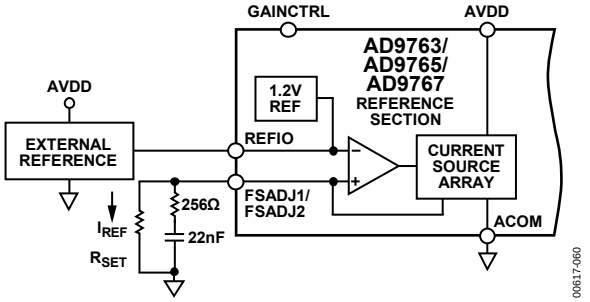


Figure 60. External Reference Configuration Gain Control Mode

GAIN CONTROL MODE

The AD9763/AD9765/AD9767 has two gain control modes, independent and master/slave. If the GAINCTRL terminal is low (connected to ground), the full-scale currents of DAC1 and DAC2 are set separately using two different R_{SET} resistors. One resistor is connected to the FSADJ1 terminal, and the other resistor is connected to the FSADJ2 terminal. This is independent mode. If the GAINCTRL terminal is set high (connected to AVDD), the full-scale currents of DAC1 and DAC2 are set to the same value using one R_{SET} resistor. In master/slave mode, full-scale current for both DAC1 and DAC2 is set via the FSADJ1 terminal.

SETTING THE FULL-SCALE CURRENT

Both of the DACs in the AD9763/AD9765/AD9767 contain a control amplifier that is used to regulate the full-scale output current (I_{OUTFS}). The control amplifier is configured as a V-I converter, as shown in Figure 59, so that its current output (I_{REF}) is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}.

$$I_{REF} = V_{REFIO}/R_{SET}$$

The DAC full-scale current, I_{OUTFS}, is an output current 32 times larger than the reference current, I_{REF}.

$$I_{OUTFS} = 32 \times I_{REF}$$

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} from 2 mA to 20 mA by setting I_{REF} between 62.5 µA and 625 µA. The wide adjustment range of I_{OUTFS} provides several benefits. The first relates directly to the power dissipation of the AD9763/AD9765/AD9767, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second relates to the 20 dB adjustment, which is useful for system gain control purposes.

To ensure that the AD9763/AD9765/AD9767 performs properly, connect a 22 nF capacitor and 256 Ω resistor network (shown in Figure 59 and Figure 60) from the FSADJ1 terminal to ground and from the FSADJ2 terminal to ground.

DAC TRANSFER FUNCTION

Both DACs in the AD9763/AD9765/AD9767 provide complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} provides a near full-scale current output (I_{OUTFS}) when all bits are high (that is, DAC CODE = 1024/4095/16,384 for the AD9763/AD9765/AD9767, respectively), while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS}. I_{OUTA} for the AD9763, AD9765, and AD9767, respectively, can be expressed as

$$I_{OUTA} = (DAC\ CODE/1024) \times I_{OUTFS} \quad (1)$$

$$I_{OUTA} = (DAC\ CODE/4096) \times I_{OUTFS}$$

$$I_{OUTA} = (DAC\ CODE/16{,}384) \times I_{OUTFS}$$

I_{OUTB} for the AD9763, AD9765, and AD9767, respectively, can be expressed as

$$I_{OUTB} = ((1023 - DAC\ CODE)/1024) \times I_{OUTFS} \quad (2)$$

$$I_{OUTB} = ((4095 - DAC\ CODE)/4096) \times I_{OUTFS}$$

$$I_{OUTB} = ((16{,}383 - DAC\ CODE)/16{,}384) \times I_{OUTFS}$$

where *DAC CODE* = 0 to 1024, 0 to 4095, or 0 to 16,384 (decimal representation).

I_{OUTFS} is a function of the reference current (I_{REF}). This is nominally set by a reference voltage (V_{REFIO}) and an external resistor (R_{SET}). It can be expressed as

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where I_{REF} is set as discussed in the Setting the Full-Scale Current section.

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads (R_{LOAD}) that are tied to the analog common (ACOM). Note that R_{LOAD} can represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB}, as is the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} must not exceed the specified output compliance range to maintain the specified distortion and linearity performance.

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Equation 7 highlights some of the advantages of operating the AD9763/AD9765/AD9767 differentially. First, the differential operation helps cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion, and dc offsets. Second, the differential code-dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (that is, V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

The gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9763/AD9765/AD9767 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship.

ANALOG OUTPUTS

The complementary current outputs, I_{OUTA} and I_{OUTB}, in each DAC can be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor (R_{LOAD}) as described in Equation 5 through Equation 7. The differential voltage (V_{DIFF}) existing between V_{OUTA} and V_{OUTB} can be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9763/AD9765/AD9767 is optimum and specified using a differential transformer-coupled output in which the voltage swing at I_{OUTA} and I_{OUTB} is limited to ±0.5 V. If a single-ended unipolar output is desired, select IOUTA.

The distortion and noise performance of the AD9763/AD9765/AD9767 can be enhanced when it is configured for differential operation. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first-order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load, assuming no source termination. Because the output currents of I_{OUTA} and I_{OUTB} are complementary, they become additive when processed differentially. A properly selected transformer allows the AD9763/AD9765/AD9767 to provide the required power and voltage levels to different loads.

The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 kΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (that is, V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground via an I-V op amp configuration results in the optimum dc linearity. Note that the INL/DNL specifications for the AD9763/AD9765/AD9767 are measured with I_{OUTA} maintained at a virtual ground via an op amp.

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of −1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9763/AD9765/AD9767.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. When I_{OUTFS} is decreased from 20 mA to 2 mA, the positive output compliance range degrades slightly from its nominal 1.25 V to 1.00 V. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed 0.5 V. Applications requiring the AD9763/AD9765/AD9767 output (that is, V_{OUTA} and/or V_{OUTB}) to extend its output compliance range must size R_{LOAD} accordingly. Operation beyond this compliance range adversely affects the linearity performance of the AD9763/AD9765/AD9767 and subsequently degrades its distortion performance.

DIGITAL INPUTS

The digital inputs of the AD9763/AD9765/AD9767 consist of two independent channels. For the dual-port mode, each DAC has its own dedicated 10-/12-/14-bit data port: WRT line and CLK line. In the interleaved timing mode, the function of the digital control pins changes as described in the Interleaved Mode Timing section. The 10-/12-/14-bit parallel data inputs follow straight binary coding, where the most significant bits (MSBs) are DB9P1 and DB9P2 for the AD9763, DB11P1 and DB11P2 for the AD9765, and DB13P1 and DB13P2 for the AD9767, and the least significant bits (LSBs) are DB0P1 and DB0P2 for all three parts. I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master/slave latch. The DAC outputs are updated following either the rising edge or every other rising edge of the clock, depending on whether dual or interleaved mode is used. The DAC outputs are designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse width. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

DAC TIMING

The AD9763/AD9765/AD9767 can operate in two timing modes, dual and interleaved, which are described in the following sections. The block diagram in Figure 61 represents the latch architecture in the interleaved timing mode.

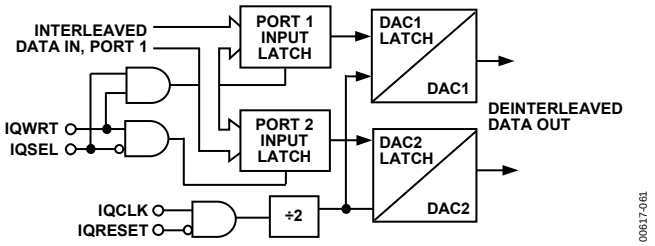


Figure 61. Latch Structure in Interleaved Mode

Dual-Port Mode Timing

When the MODE pin is at Logic 1, the AD9763/AD9765/AD9767 operates in dual-port mode (refer to Figure 57). The AD9763/AD9765/AD9767 functions as two distinct DACs. Each DAC has its own completely independent digital input and control lines.

The AD9763/AD9765/AD9767 features a double-buffered data path. Data enters the device through the channel input latches. This data is then transferred to the DAC latch in each signal path. After the data is loaded into the DAC latch, the analog output settles to its new value.

For general consideration, the WRT lines control the channel input latches, and the CLK lines control the DAC latches. Both sets of latches are updated on the rising edge of their respective control signals.

The rising edge of CLK must occur before or simultaneously with the rising edge of WRT. If the rising edge of CLK occurs after the rising edge of WRT, a minimum delay of 2 ns must be maintained from the rising edge of WRT to the rising edge of CLK.

Timing specifications for dual-port mode are shown in Figure 62 and Figure 63.

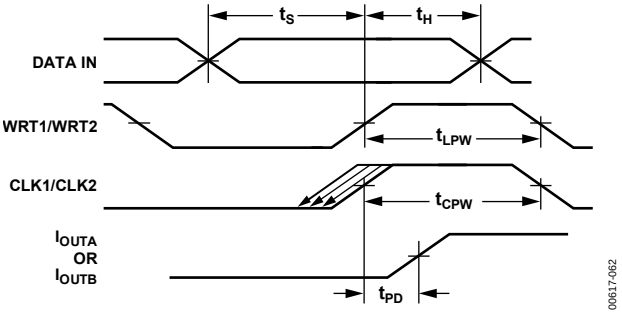


Figure 62. Dual-Port Mode Timing

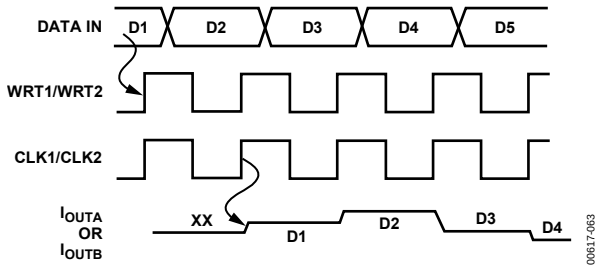


Figure 63. Dual-Port Mode Timing

Interleaved Mode Timing

When the MODE pin is at Logic 0, the AD9763/AD9765/AD9767 operate in interleaved mode (refer to Figure 61). In addition, WRT1 functions as IQWRT, CLK1 functions as IQCLK, WRT2 functions as IQSEL, and CLK2 functions as IQRESET.

Data enters the device on the rising edge of IQWRT. The logic level of IQSEL steers the data to either Channel Latch 1 (IQSEL = 1) or to Channel Latch 2 (IQSEL = 0). For proper operation, IQSEL must change state only when IQWRT and IQCLK are low.

When IQRESET is high, IQCLK is disabled. When IQRESET goes low, the next rising edge on IQCLK updates both DAC latches with the data present at their inputs. In the interleaved mode, IQCLK is divided by 2 internally. Following this first rising edge, the DAC latches are only updated on every other rising edge of IQCLK. In this way, IQRESET can be used to synchronize the routing of the data to the DACs.

Similar to the order of CLK and WRT in dual-port mode, IQCLK must occur before or simultaneously with IQWRT.

Timing specifications for interleaved mode are shown in Figure 64 and Figure 66.

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (DVDDx), or

$$V_{THRESHOLD} = DVDDx/2(\pm 20\%)$$

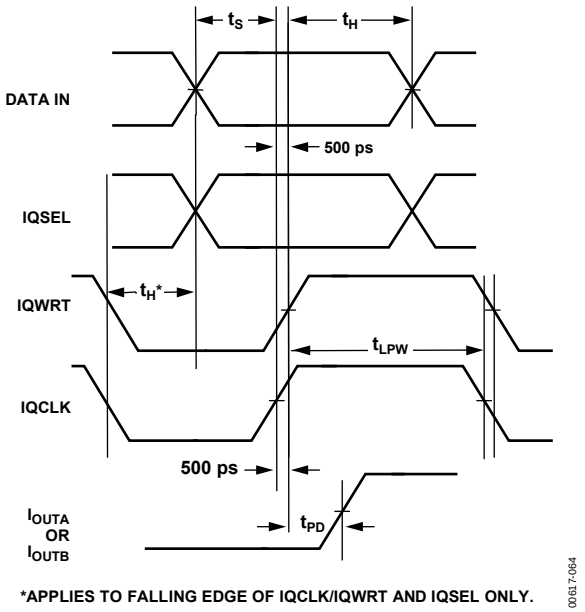


Figure 64. 5 V or 3.3 V Interleaved Mode Timing

At 5 V it is permissible to drive IQWRT and IQCLK together as shown in Figure 65, but at 3.3 V the interleaved data transfer is not reliable.

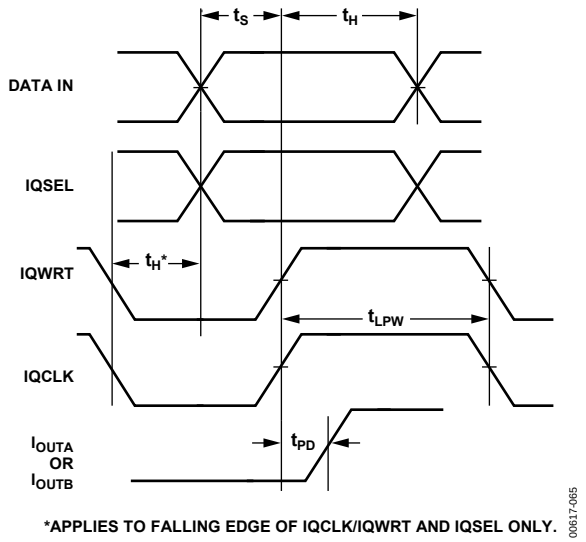


Figure 65. 5 V Only Interleaved Mode Timing

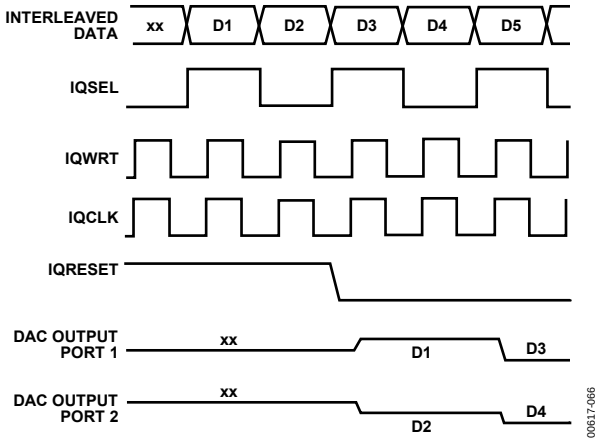


Figure 66. Interleaved Mode Timing

The internal digital circuitry of the AD9763/AD9765/AD9767 is capable of operating at a digital supply of 3.3 V or 5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD1/DVDD2 is set to accommodate the maximum high level voltage ($V_{OH(MAX)}$) of the TTL drivers. A DVDD1/DVDD2 of 3.3 V typically ensures proper compatibility with bipolar TTL logic families. Figure 67 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar, with the exception that it contains an active pull-down circuit, thus ensuring that the AD9763/AD9765/AD9767 remains enabled if this input is left disconnected.

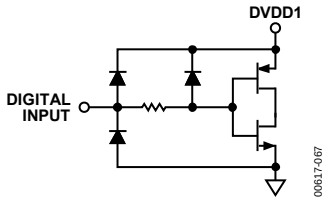


Figure 67. Equivalent Digital Input

Because the AD9763/AD9765/AD9767 is capable of being clocked up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. Operating the AD9763/AD9765/AD9767 with reduced logic swings and a corresponding digital supply (DVDD1/DVDD2) results in the lowest data feedthrough and on-chip digital noise. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the AD9763/AD9765/AD9767 as well as its required minimum and maximum input logic level thresholds.

Digital signal paths should be kept short, and run lengths should be matched to avoid propagation delay mismatch. The insertion of a low value (that is, 20 Ω to 100 Ω) resistor network between the AD9763/AD9765/AD9767 digital inputs and driver outputs can be helpful in reducing any overshooting and ringing at the digital inputs that contribute to digital feedthrough. For longer board traces and high data update rates, stripline techniques with proper impedance and termination resistors should be considered to maintain "clean" digital inputs.

The external clock driver circuitry provides the AD9763/AD9765/AD9767 with a low-jitter clock input meeting the minimum and maximum logic levels while providing fast edges. Fast clock edges help minimize jitter manifesting itself as phase noise on a reconstructed waveform. Therefore, the clock input should be driven by the fastest logic family suitable for the application.

Note that the clock input can also be driven via a sine wave, which is centered around the digital threshold (that is, DVDDx/2) and meets the minimum and maximum logic threshold. This typically results in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. In addition, at higher sampling rates, the 20% tolerance of the digital logic threshold should be considered, because it affects the effective clock duty cycle and, subsequently, cuts into the required data setup and hold times.

Input Clock and Data Timing Relationship

SNR in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9763/AD9765/AD9767 are rising edge triggered and therefore exhibit SNR sensitivity when the data transition is close to this edge. The goal when applying the AD9763/AD9765/AD9767 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 68 shows the relationship of SNR to clock placement with different sample rates. Note that at the lower sample rates, much more tolerance is allowed in clock placement; much more care must be taken at higher rates.

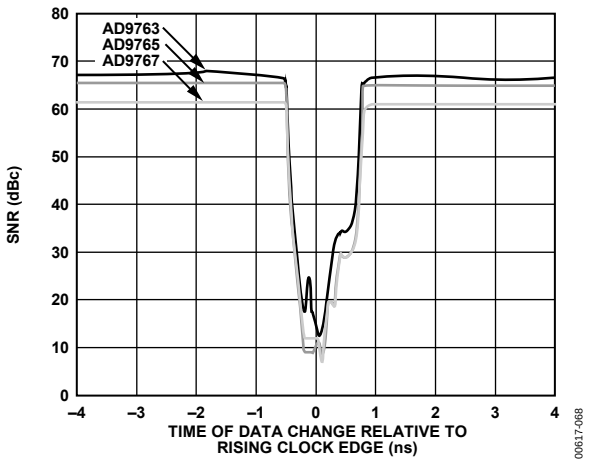


Figure 68. SNR vs. Clock Placement @ f_{OUT} = 20 MHz and f_{CLK} = 125 MSPS

SLEEP MODE OPERATION

The AD9763/AD9765/AD9767 has a power-down function that turns off the output current and reduces the supply current to less than 8.5 mA over the specified supply range of 3.3 V to 5 V and over the full operating temperature range. This mode can be activated by applying a Logic Level 1 to the SLEEP pin. The SLEEP pin logic threshold is equal to 0.5 × AVDD. This digital input also contains an active pull-down circuit that ensures the AD9763/AD9765/AD9767 remains enabled if this input is left disconnected. The AD9763/AD9765/AD9767 require less than 50 ns to power down and approximately 5 µs to power back up.

POWER DISSIPATION

The power dissipation (P_D) of the AD9763/AD9765/AD9767 is dependent on several factors, including

- the power supply voltages (AVDD and DVDD1/DVDD2)
- the full-scale current output (I_{OUTFS})
- the update rate (f_{CLK})
- the reconstructed digital input waveform

The power dissipation is directly proportional to the analog supply current (I_{AVDD}) and the digital supply current (I_{DVDD}). I_{AVDD} is directly proportional to $I_{OUTFS,}$ as shown in Figure 69, and is insensitive to f_{CLK}.

Conversely, I_{DVDD} is dependent on the digital input waveform, the f_{CLK}, and the digital supply (DVDD1/DVDD2). Figure 70 and Figure 71 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLK}) for various update rates with DVDD1 = DVDD2 = 5 V and DVDD1 = DVDD2 = 3.3 V, respectively. Note that I_{DVDD} is reduced by more than a factor of 2 when DVDD1/DVDD2 is reduced from 5 V to 3.3 V.

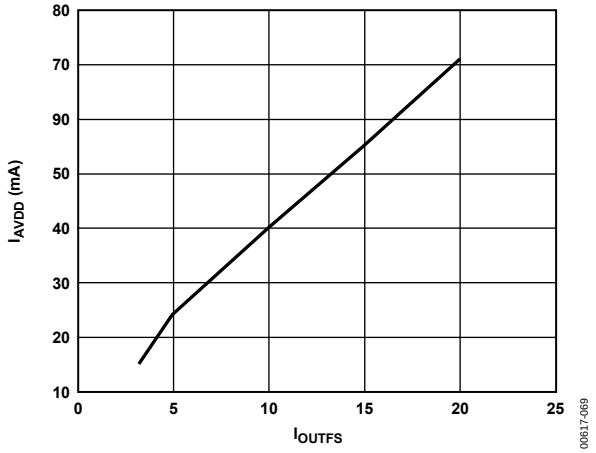


Figure 69. I_{AVDD} vs. I_{OUTFS}

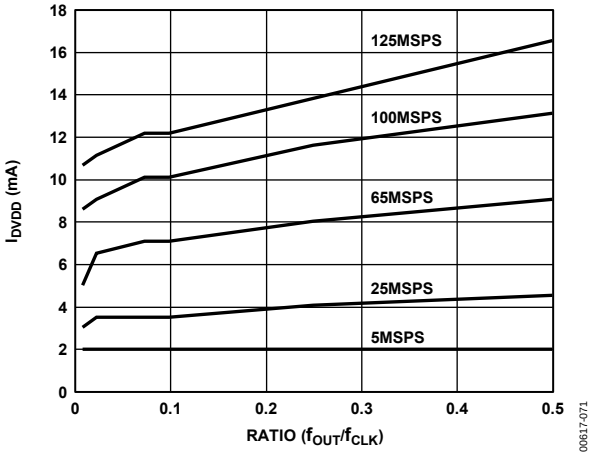


Figure 71. I_{DVDD} vs. Ratio @ DVDD1 = DVDD2 = 3.3 V

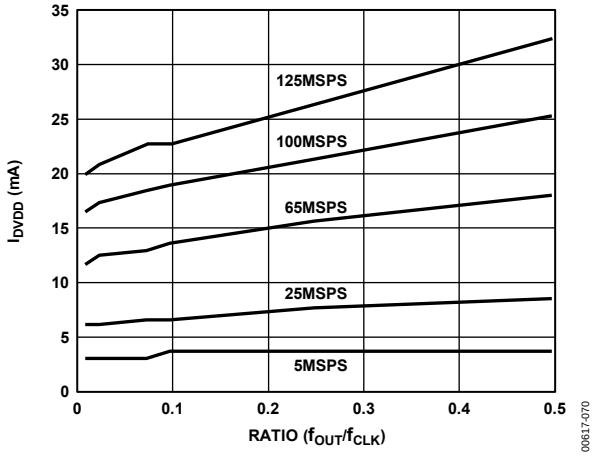


Figure 70. I_{DVDD} vs. Ratio @ DVDD1 = DVDD2 = 5 V

APPLYING THE AD9763/AD9765/AD9767

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9763/AD9765/AD9767, with I_{OUTFS} set to a nominal 20 mA, unless otherwise noted. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, bipolar output, signal gain, and/or level shifting within the bandwidth of the chosen op amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage results if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor (R_{LOAD}) referred to as ACOM. This configuration may be more suitable for a single-supply system requiring a dc-coupled, ground-referred output voltage. Alternatively, an amplifier can be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity because I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note that I_{OUTA} provides slightly better performance than I_{OUTB}.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used as shown in Figure 72 to perform a differential-to-single-ended signal conversion. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the pass band of the transformer. An RF transformer such as the Mini-Circuits® T1-1T provides excellent rejection of common-mode distortion (that is, even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios can also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

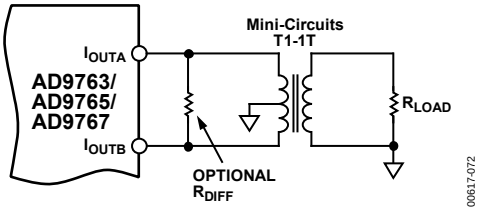


Figure 72. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (that is, V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and must be maintained with the output compliance range of the AD9763/AD9765/AD9767 to achieve the specified performance. A differential resistor (R_{DIFF}) can be inserted in applications where the output of the transformer is connected to the load (R_{LOAD}) via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used as shown in Figure 73 to perform a differential-to-single-ended conversion. The AD9763/AD9765/AD9767 is configured with two equal load resistors (R_{LOAD}) of 25 Ω each. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor often enhances the op amp's distortion performance by preventing the DAC's high-slewing output from overloading the op amp's input.

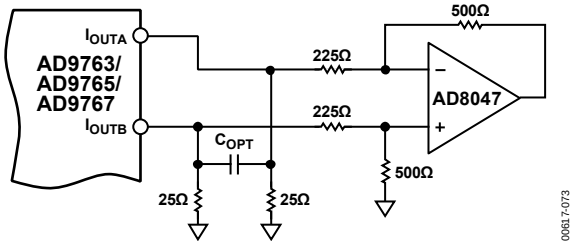


Figure 73. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate from a dual supply because its output is approximately ±1.0 V. Select a high speed amplifier capable of preserving the differential performance of the AD9763/AD9765/AD9767 while meeting other system level objectives (that is, cost or power). Consider the op amp's differential gain, gain setting resistor values, and full-scale output swing capabilities when optimizing this circuit.

The differential circuit shown in Figure 74 provides the necessary level shifting required in a single-supply system. In this case, AVDD, which is the positive analog supply for both the AD9763/AD9765/AD9767 and the op amp, is used to level shift the differential output of the AD9763/AD9765/AD9767 to midsupply (that is, AVDD/2). The AD8055 is a suitable op amp for this application.

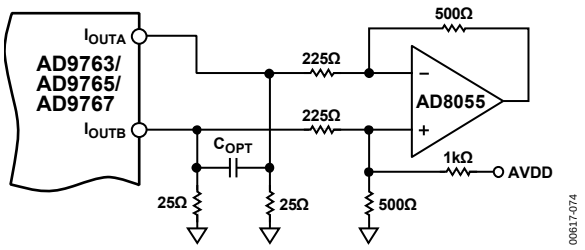


Figure 74. Single-Supply DC Differential-Coupled Circuit

SINGLE-ENDED, UNBUFFERED VOLTAGE OUTPUT

Figure 75 shows the AD9763/AD9765/AD9767 configured to provide a unipolar output range of approximately 0 V to 0.5 V for a doubly terminated 50 Ω cable, because the nominal full-scale current (I_{OUTFS}) of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB}. The unused output (I_{OUTA} or I_{OUTB}) can be connected directly to ACOM or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the INL (see the Analog Outputs section). For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

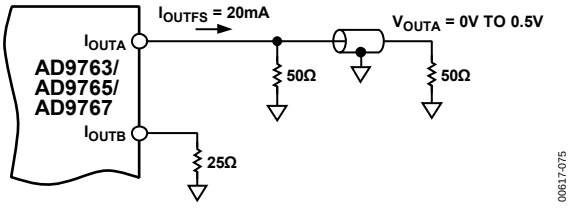


Figure 75. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 76 shows a buffered single-ended output configuration in which the U1 op amp performs an I-V conversion on the AD9763/AD9765/AD9767 output current. U1 maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the INL performance of the DAC, as described in the Analog Outputs section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by the slewing capabilities of U1. U1 provides a negative unipolar output voltage, and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. Set the full-scale output within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} because the signal current U1 has to sink will be subsequently reduced.

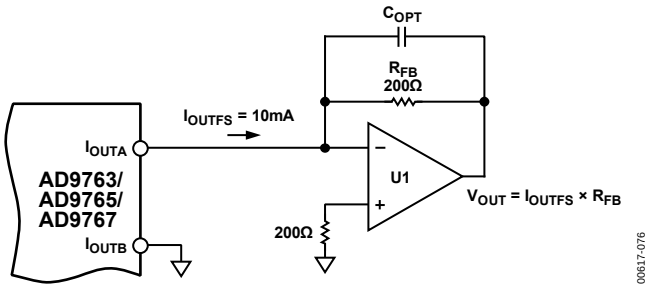


Figure 76. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS

Power Supply Rejection

Many applications seek high speed and high performance under less than ideal operating conditions. In these applications, the implementation and construction of the printed circuit board is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing as well as power supply bypassing and grounding to ensure optimum performance. Figure 92 to Figure 93 illustrate recommended printed circuit board ground, power, and signal plane layouts that are implemented on the AD9763/AD9765/AD9767 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution. This is referred to as the power supply rejection ratio (PSRR). For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full-scale current, I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise occurs over the spectrum of tens of kilohertz to several megahertz. The PSRR vs. frequency of the AD9763/AD9765/AD9767 AVDD supply over this frequency range is shown in Figure 77.

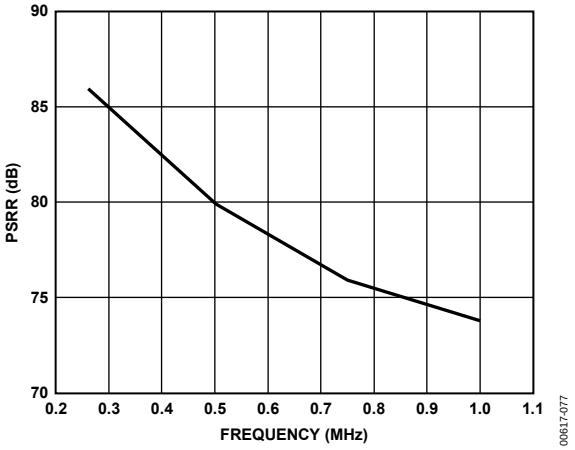


Figure 77. AVDD Power Supply Rejection Ratio vs. Frequency

Note that the data in Figure 77 is given in terms of current out vs. voltage in. Noise on the analog power supply has the effect of modulating the internal current sources and therefore the output current. The voltage noise on AVDD, therefore, is added in a nonlinear manner to the desired I_{OUT}. PSRR is very code dependent, thus producing mixing effects that can modulate low frequency power supply noise to higher frequencies. Worst-case PSRR for either one of the differential DAC outputs occurs when the full-scale current is directed toward that output. As a result, the PSRR measurement in Figure 77 represents a worst-case condition in which the digital inputs remain static and the full-scale output current of 20 mA is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV of noise and, for simplicity's sake, all of this noise is concentrated at 250 kHz (that is, ignore harmonics). To calculate how much of this undesired noise will appear as current noise superimposed on the DAC full-scale current, I_{OUTFS}, one must determine the PSRR in decibels using Figure 77 at 250 kHz. To calculate the PSRR for a given R_{LOAD}, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 77 by the scaling factor $20 \times \log(R_{LOAD})$. For example, if R_{LOAD} is 50 Ω, the PSRR is reduced by 34 dB (that is, the PSRR of the DAC at 250 kHz, which is 85 dB in Figure 77, becomes 51 dB V_{OUT}/V_{IN}).

Proper grounding and decoupling are primary objectives in any high speed, high resolution system. The AD9763/AD9765/AD9767 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, decouple the analog supply (AVDD) to the analog common (ACOM) as close to the chip as physically possible. Similarly, decouple the digital supply (DVDD1/DVDD2) to the digital common (DCOM1/DCOM2) as close to the chip as possible.

For those applications that require a single 5 V or 3.3 V supply for both the analog and digital supplies, a clean analog supply can be generated using the circuit shown in Figure 78. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained by using low-ESR type electrolytic and tantalum capacitors.

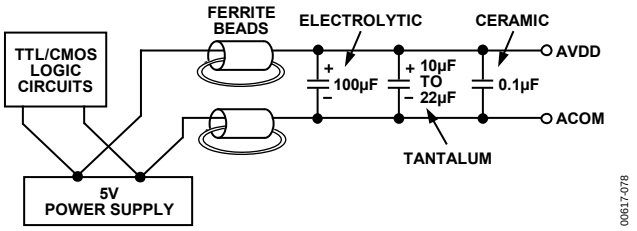


Figure 78. Differential LC Filter for Single 5 V and 3.3 V Applications

APPLICATIONS INFORMATION

VDSL EXAMPLE APPLICATIONS USING THE AD9765 AND AD9767

Very high frequency digital subscriber line (VDSL) technology is growing rapidly in applications requiring data transfer over relatively short distances. By using quadrature amplitude modulation (QAM) and transmitting the data in discrete multiple tones (DMT), high data rates can be achieved.

As with other multitone applications, each VDSL tone is capable of transmitting a given number of bits, depending on the signal-to-noise ratio (SNR) in a narrow band around that tone. For a typical VDSL application, the tones are evenly spaced over the range of several kHz to 10 MHz. At the high frequency end of this range, performance is generally limited by cable characteristics and environmental factors such as external interferers. Performance at the lower frequencies is much more dependent on the performance of the components in the signal chain. In addition to in-band noise, intermodulation from other tones can also potentially interfere with the data recovery for a given tone. The two graphs in Figure 79 and Figure 81 represent a 500-tone missing bin test vector, with frequencies evenly spaced from 400 Hz to 10 MHz. This test is very commonly done to determine if distortion limits the number of bits that can be transmitted in a tone. The test vector has a series of missing tones around 750 kHz, which is represented in Figure 79, and a series of missing tones around 5 MHz, which is represented in Figure 81. In both cases, the spurious-free dynamic range (SFDR) between the transmitted tones and the empty bins is greater than 60 dB.

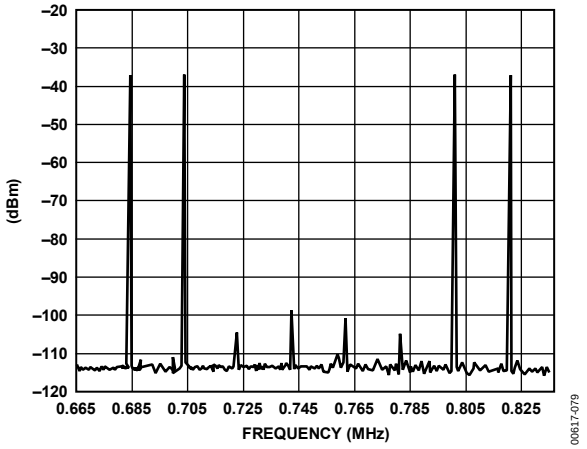


Figure 79. AD9765 Notch in Missing Bin at 750 kHz Is Down >60 dB (Peak Amplitude = 0 dBm)

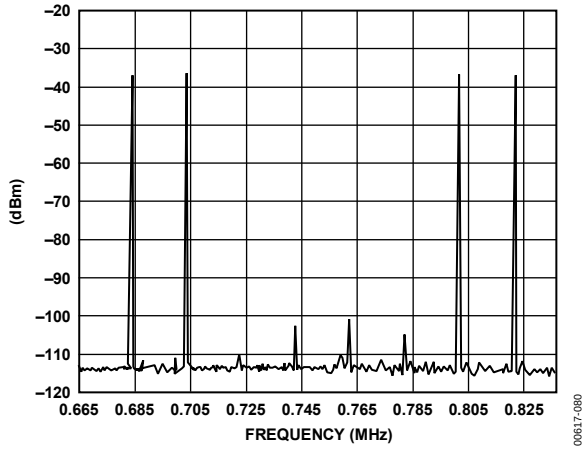


Figure 80. AD9767 Notch in Missing Bin at 750 kHz Is Down >60 dB (Peak Amplitude = 0 dBm)

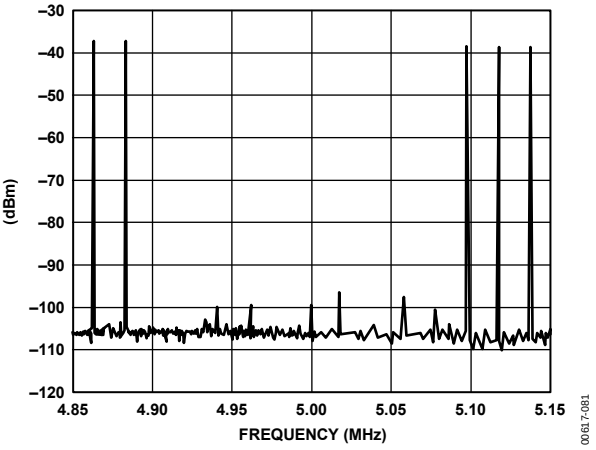


Figure 81. AD9765 Notch in Missing Bin at 5 MHz Is Down >60 dB (Peak Amplitude = 0 dBm)

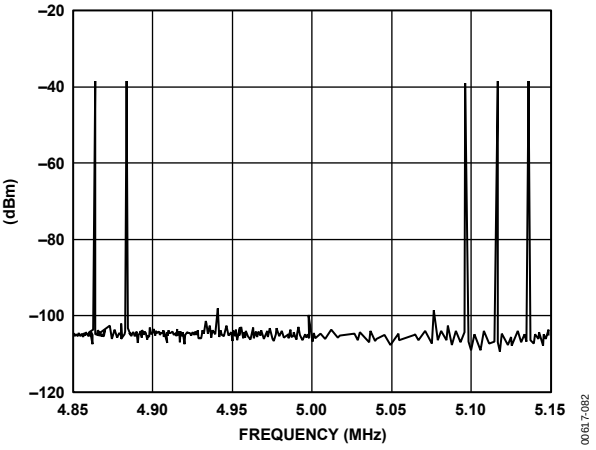


Figure 82. AD9767 Notch in Missing Bin at 5 MHz Is Down >60 dB (Peak Amplitude = 0 dBm)

QUADRATURE AMPLITUDE MODULATION (QAM) EXAMPLE USING THE AD9763

QAM is one of the most widely used digital modulation schemes in digital communications systems. This modulation technique can be found in FDM as well as spread spectrum (that is, CDMA) based systems. A QAM signal is a carrier frequency that is modulated in both amplitude (that is, AM modulation) and phase (that is, PM modulation). It can be generated by independently modulating two carriers of identical frequency but with a 90° phase difference. This results in an in-phase (I) carrier component and a quadrature (Q) carrier component at a 90° phase shift with respect to the I component. The I and Q components are then summed to provide a QAM signal at the specified carrier frequency.

A common and traditional implementation of a QAM modulator is shown in Figure 83. The modulation is performed in the analog domain in which two DACs are used to generate the baseband I and Q components. Each component is then typically applied to a Nyquist filter before being applied to a quadrature mixer. The matching Nyquist filters shape and limit each component's spectral envelope while minimizing intersymbol interference. The DAC is typically updated at the QAM symbol rate, or at a multiple of the QAM symbol rate if an interpolating filter precedes the DAC. The use of an interpolating filter typically eases the implementation and complexity of the analog filter, which can be a significant contributor to mismatches in gain and phase between the two baseband channels. A quadrature mixer modulates the I and Q components with the in-phase and quadrature carrier frequency and then sums the two outputs to provide the QAM signal.

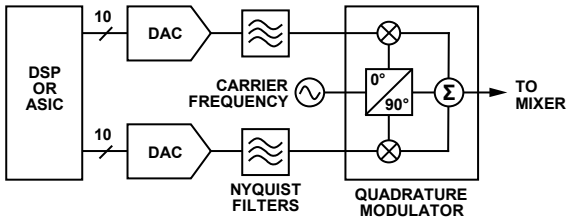


Figure 83. Typical Analog QAM Architecture

In this implementation, it is much more difficult to maintain proper gain and phase matching between the I and Q channels. The circuit implementation shown in Figure 84 helps improve the matching between the I and Q channels, and it shows a path for upconversion using the AD8346 quadrature modulator. The AD9763 provides both I and Q DACs a common reference that improves the gain matching and stability. R_{CAL} can be used to compensate for any mismatch in gain between the two channels. The mismatch can be attributed to the mismatch between R_{SET1} and R_{SET2}, the effective load resistance of each channel, and/or the voltage offset of the control amplifier in each DAC. The differential voltage outputs of both DACs in the AD9763 are fed into the respective differential inputs of the AD8346 via matching networks.

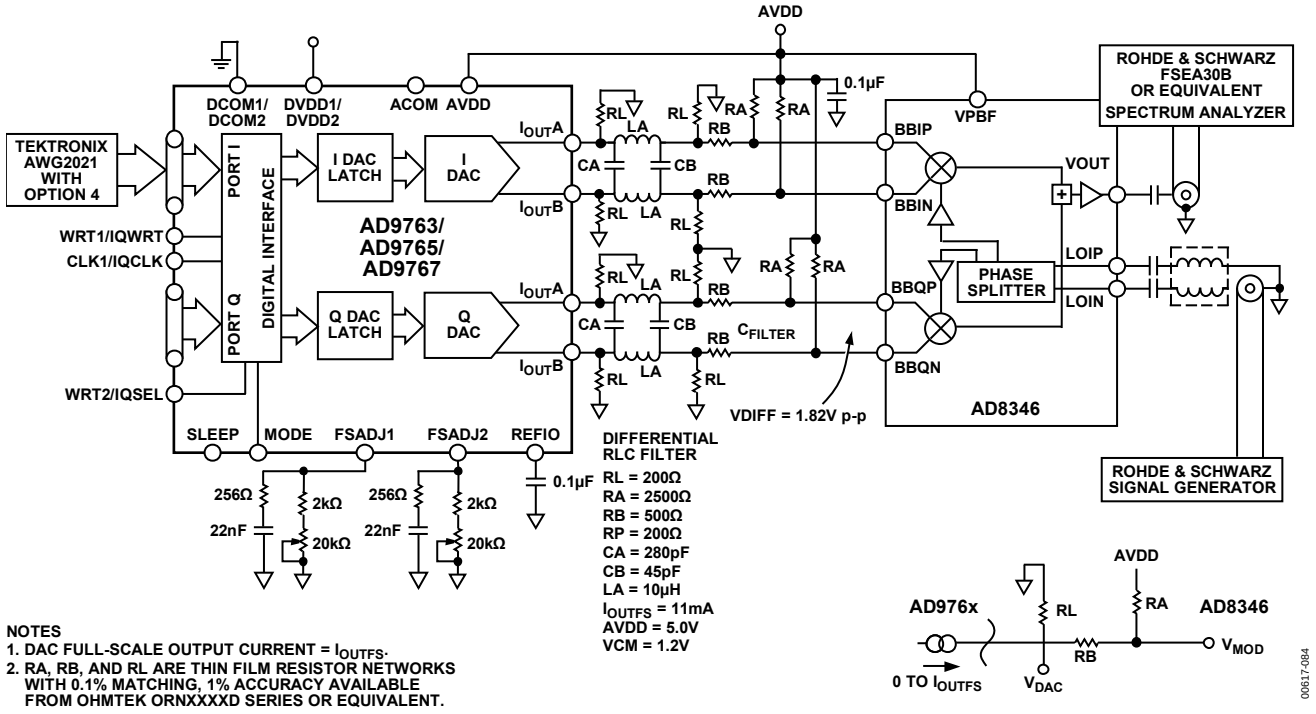


Figure 84. Baseband QAM Implementation Using an AD9763 and an AD8346

I and Q digital data can be fed into the AD9763 in two ways. In dual-port mode, the digital I information drives one input port, and the digital Q information drives the other input port. If no interpolation filter precedes the DAC, the symbol rate is the rate at which the system clock drives the CLK and WRT pins on the AD9763. In interleaved mode, the digital input stream at Port 1 contains the I and the Q information in alternating digital words. Using IQSEL and IQRESET, the AD9763 can be synchronized to the I and Q data streams. The internal timing of the AD9763 routes the selected I and Q data to the correct DAC output. In interleaved mode, if no interpolation filter precedes the AD9763, the symbol rate is half that of the system clock driving the digital data stream and the IQWRT and IQCLK pins on the AD9763.

CDMA

Code division multiple access (CDMA) is an air transmit/receive scheme in which the signal in the transmit path is modulated with a pseudorandom digital code (sometimes referred to as the spreading code). The effect of this is to spread the transmitted signal across a wide spectrum. Similar to a discrete multitone (DMT) waveform, a CDMA waveform containing multiple subscribers can be characterized as having a high peak to average ratio (that is, crest factor), thus demanding highly linear components in the transmit signal path. The bandwidth of the spectrum is defined by the CDMA standard being used, and in operation it is implemented by using a spreading code with particular characteristics.

Distortion in the transmit path can lead to power being transmitted out of the defined band. The ratio of power transmitted in-band to out-of-band is often referred to as adjacent channel power (ACP). This is a regulatory issue due to the possibility of interference with other signals being transmitted by air. Regulatory bodies define a spectral mask outside of the transmit band, and the ACP must fall under this mask. If distortion in the transmit path causes the ACP to be above the spectral mask, filtering or different component selection is needed to meet the mask requirements.

Figure 85 shows the results of using the AD9763/AD9765/AD9767 with the AD8346 to reconstruct a wideband CDMA signal centered at 2.4 GHz. The baseband signal is sampled at 65 MSPS and has a chip rate of 8 MHz.

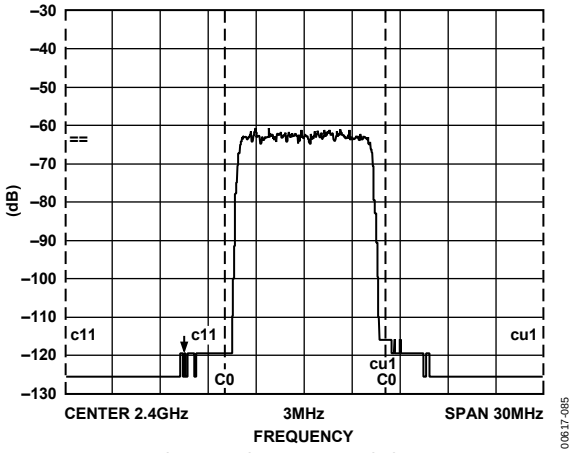


Figure 85. CDMA Signal, 8 MHz Chip Rate Sampled at 65 MSPS, Recreated at 2.4 GHz, Adjacent Channel Power >60 dBm

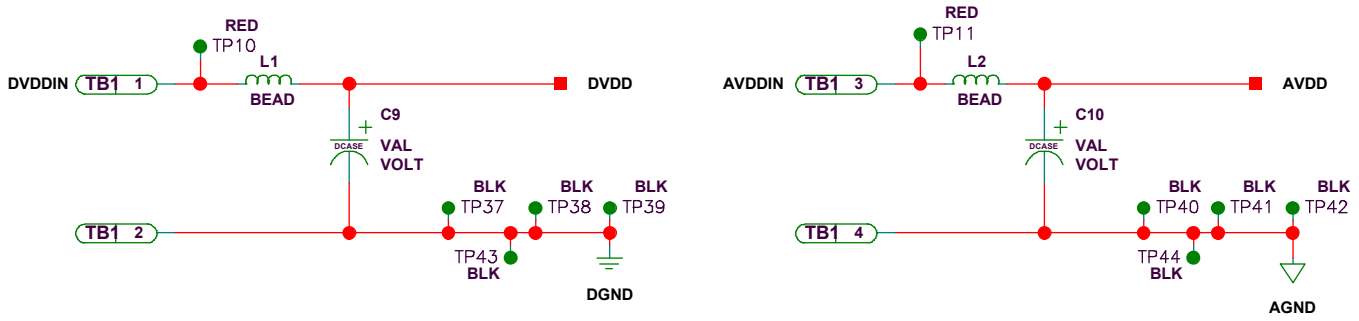
EVALUATION BOARD

GENERAL DESCRIPTION

The AD9763/AD9765/AD9767-EBZ is an evaluation board for the AD9763/AD9765/AD9767 10-/12-/14-bit dual DAC. Careful attention to layout and circuit design, combined with a prototyping area, allow the user to easily and effectively evaluate the AD9763/AD9765/AD9767 in any application where a high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9763/AD9765/AD9767 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single-ended and differential outputs. The digital inputs can be used in dual-port or interleaved mode and are designed to be driven from various word generators, with the on-board option to add a resistor network for proper load termination. When operating the AD9763/AD9765/AD9767, best performance is obtained by running the digital supply (DVDD1/DVDD2) at 3.3 V and the analog supply (AVDD) at 5 V.

SCHEMATICS



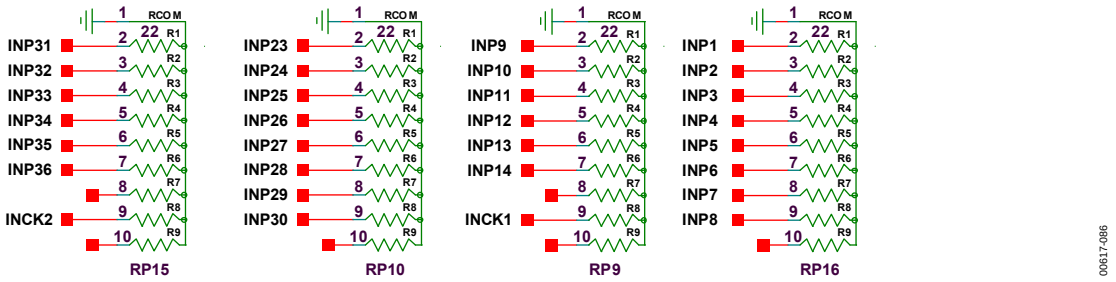


Figure 86. Power Decoupling and Clocks on AD9763/AD9765/AD9767 Evaluation Board (1)

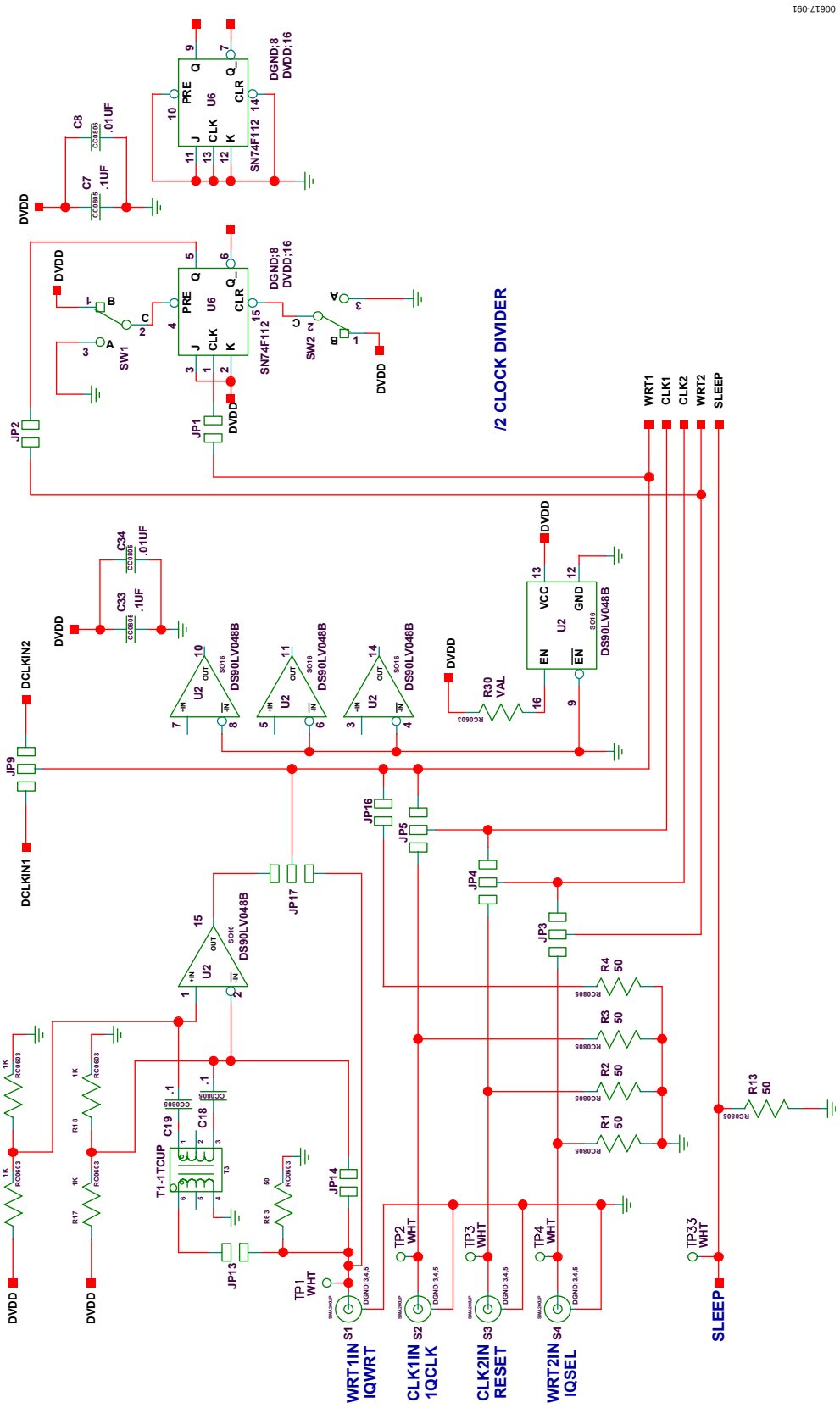


Figure 87. Power Decoupling and Clocks on AD9763/AD9765/AD9767 Evaluation Board (2)

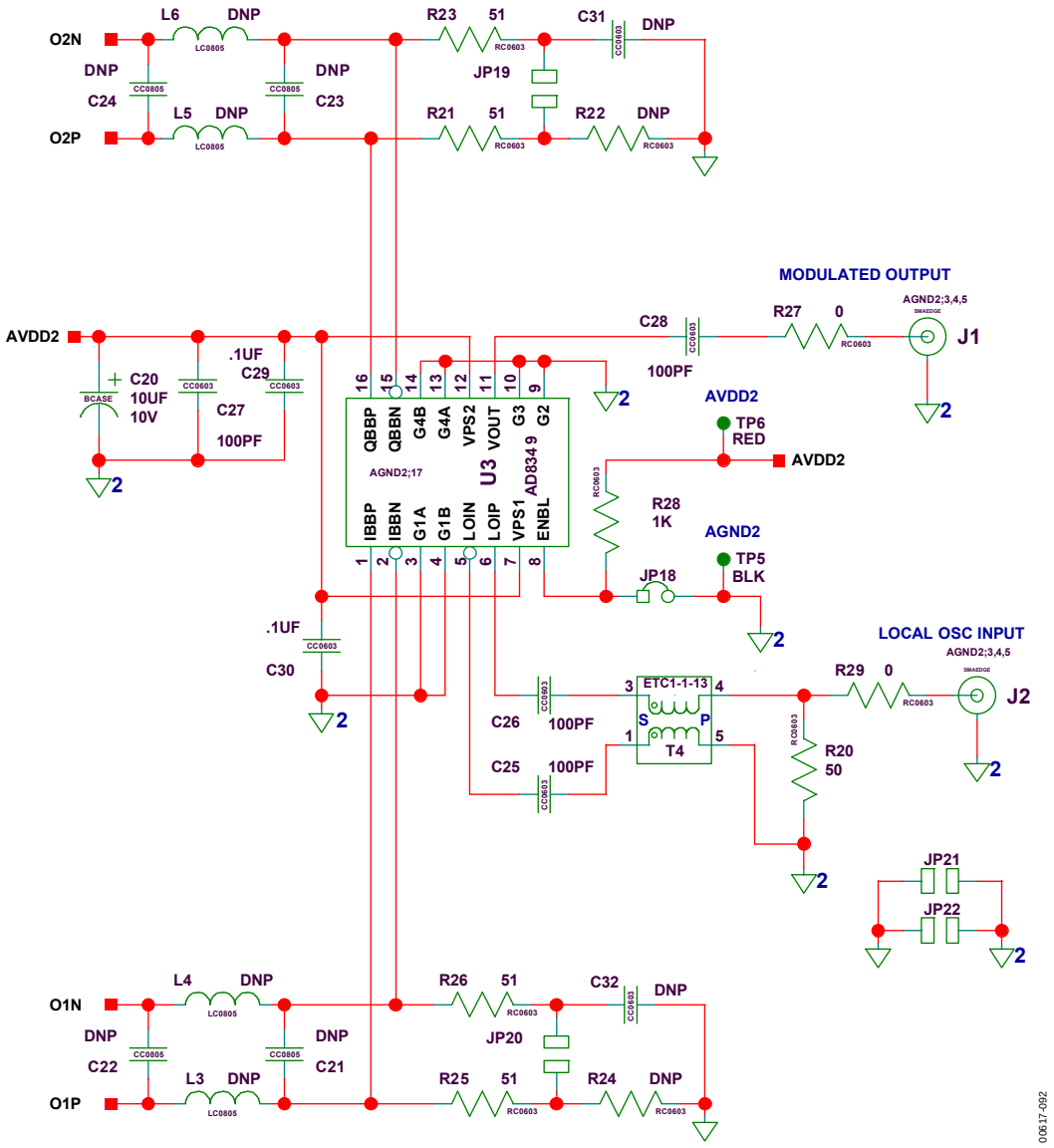


Figure 88. Modulator on AD9763/AD9765/AD9767 Evaluation Board

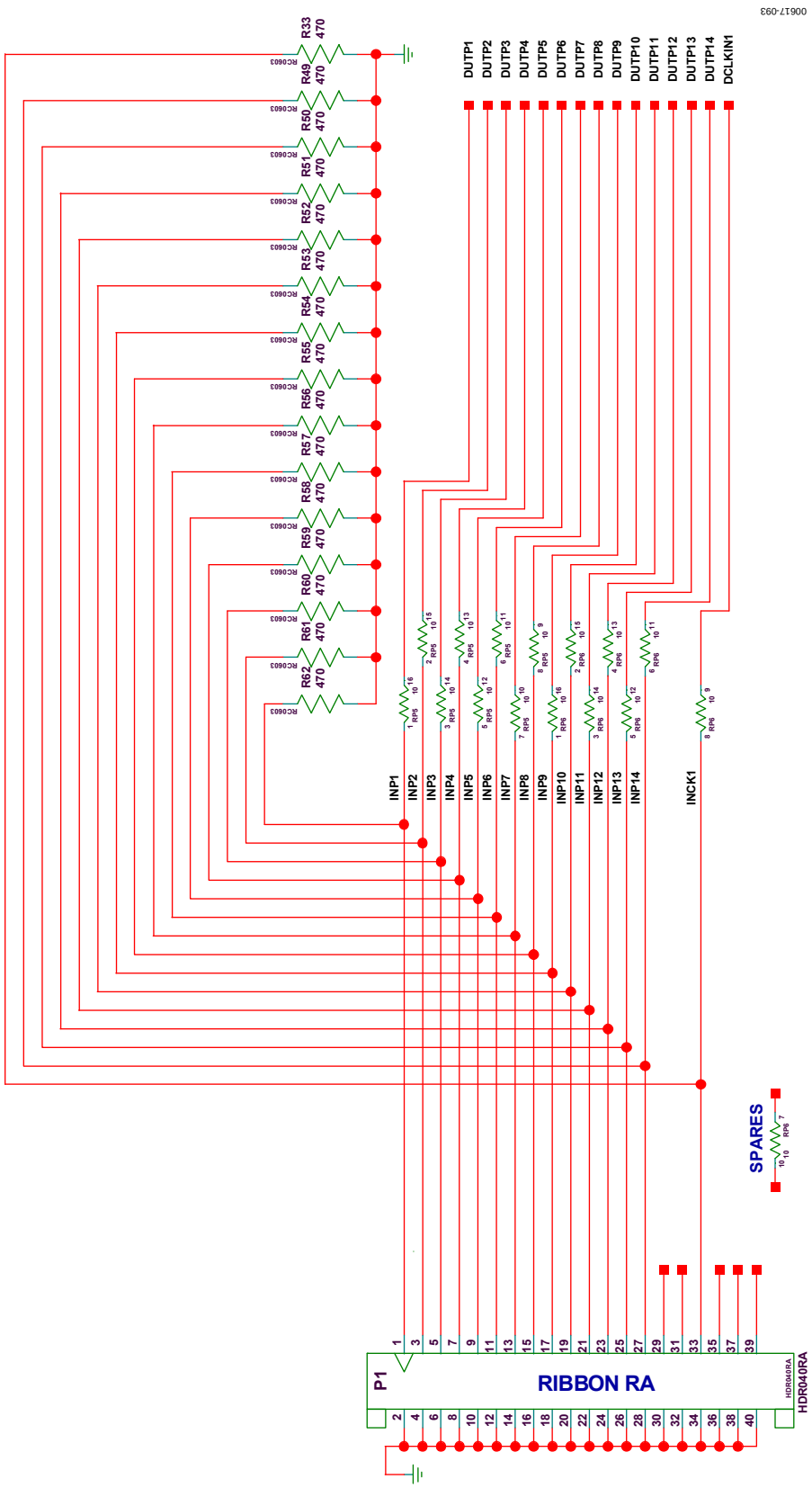


Figure 89. Digital Input Signaling (1)

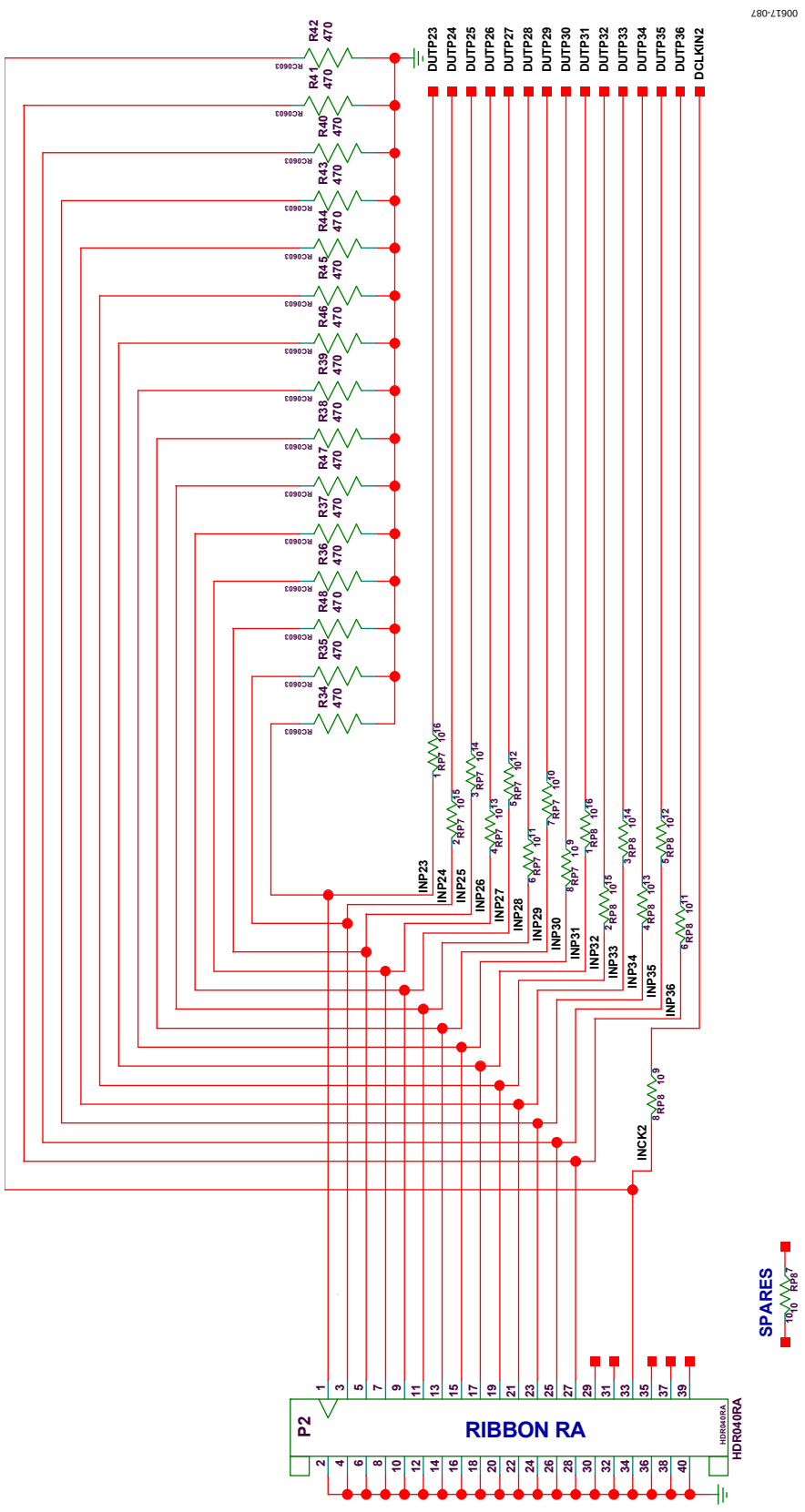


Figure 90. Digital Input Signaling (2)

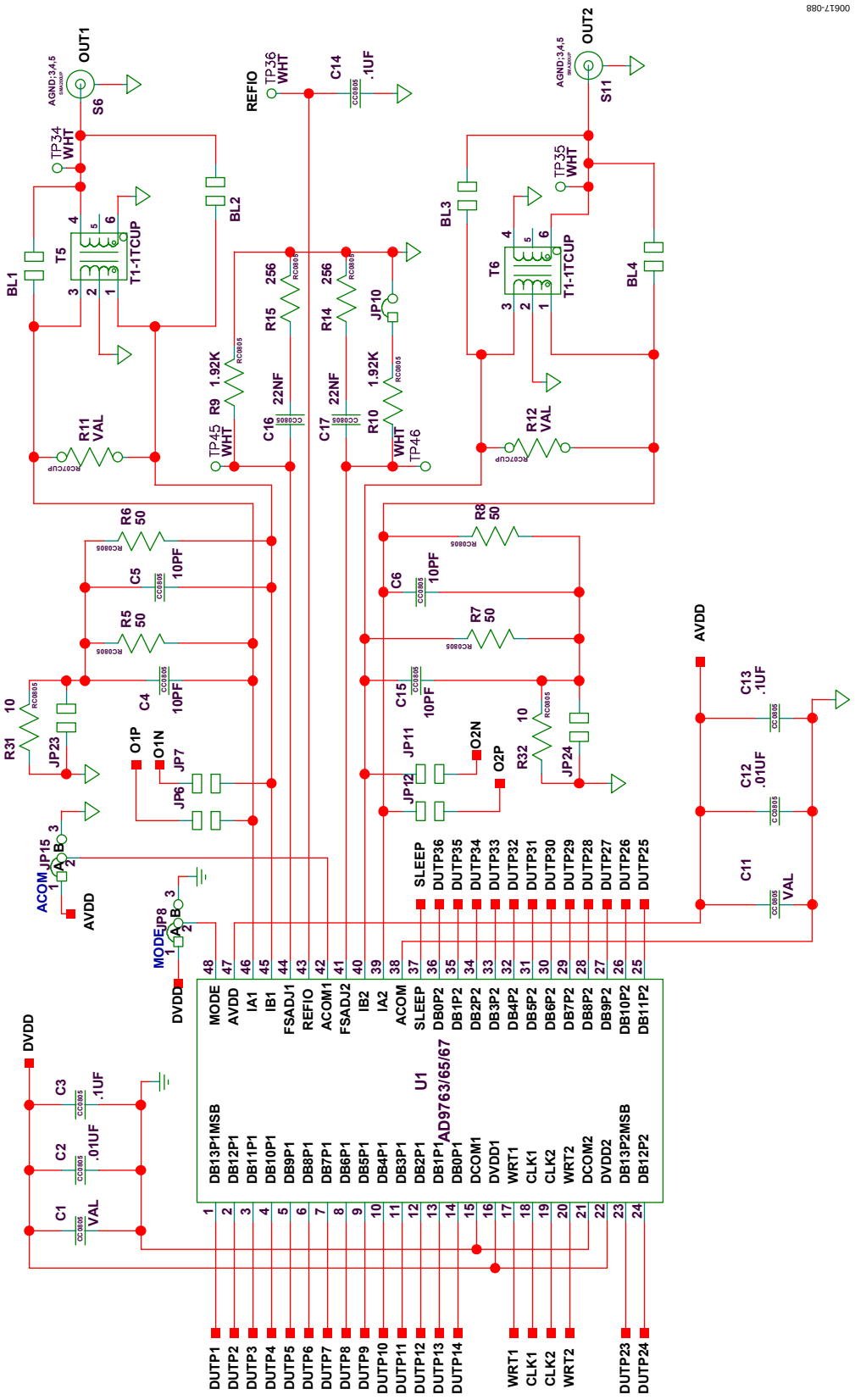


Figure 91. Device Under Test/Analog Output Signal Conditioning

EVALUATION BOARD LAYOUT

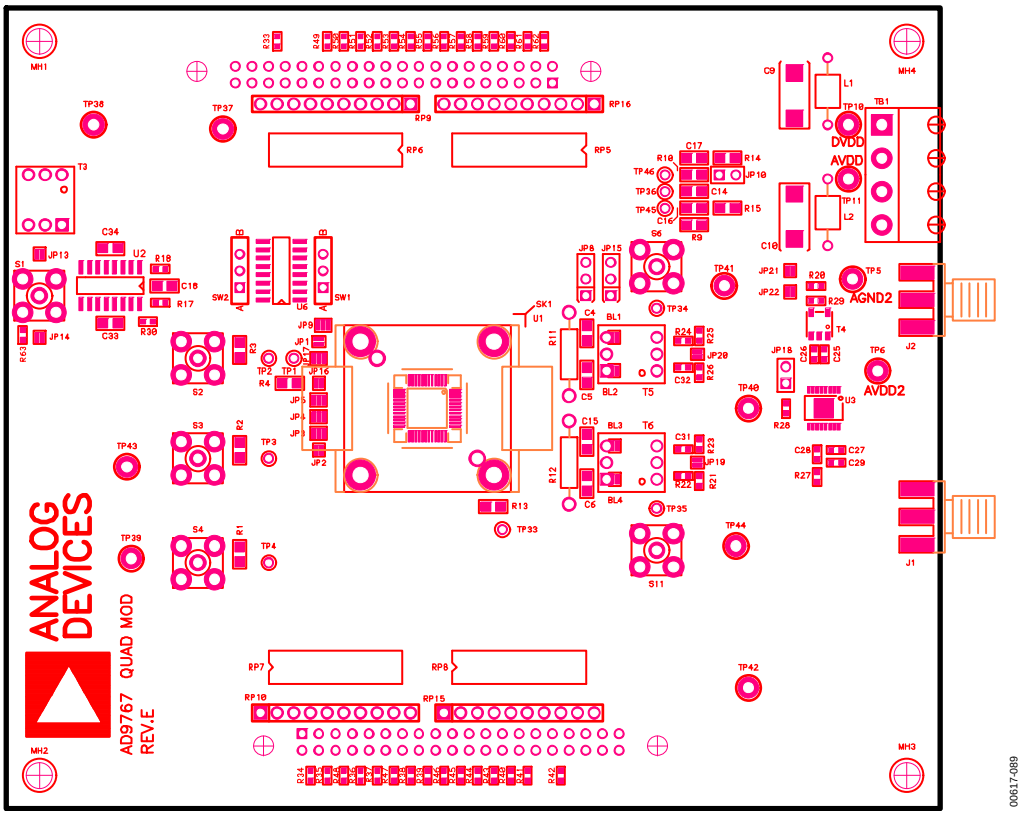


Figure 92. Assembly, Top Side

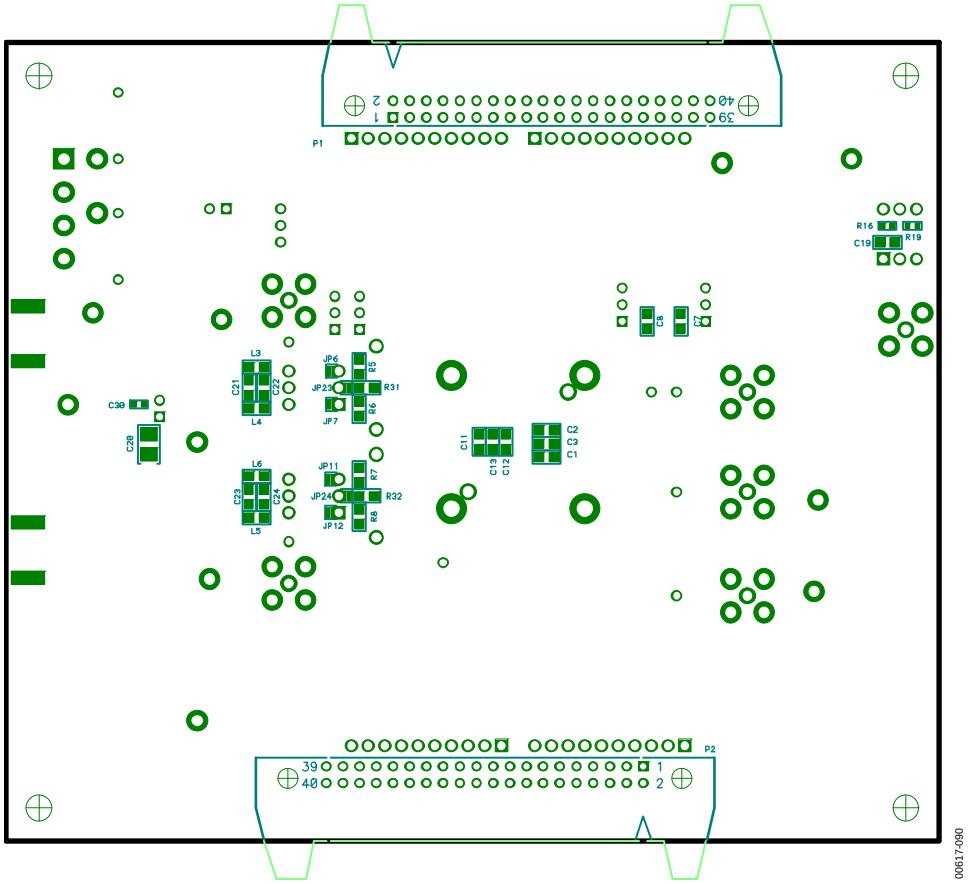


Figure 93. Assembly, Bottom Side

OUTLINE DIMENSIONS

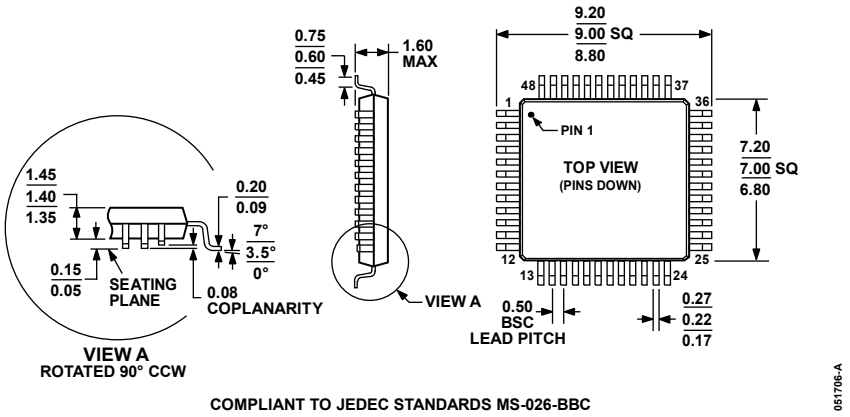


Figure 94. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9763ASTZ	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9763ASTZRL	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9763-EBZ		Evaluation Board	
AD9765AST	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9765ASTRL	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9765ASTZ	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9765ASTZRL	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9765-EBZ		Evaluation Board	
AD9767ASTZ	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9767ASTZRL	–40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD9767-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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